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UNIVERSITI TEKNOLOGI PETRONAS

DESIGN OF A GAAS DISTRIBUTED AMPLIFIER WITH LC TRAPS BASED BROADBAND LINEARIZATION

by

KOH MINGHAO

The undersigned certify that they have read, and recommend to the Postgraduate Studies Programme for acceptance this thesis for the fulfilment of the requirements for the degree stated.

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Date: _____

DESIGN OF A GAAS DISTRIBUTED AMPLIFIER WITH LC TRAPS BASED BROADBAND LINEARIZATION

by

KOH MINGHAO

A Thesis

Submitted to the Postgraduate Studies Programme

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AUGUST 2010

DECLARATION OF THESIS

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I, KOH MINGHAO
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hereby declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UTP or other institutions.

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To My Beloved Parents

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Minghao

ABSTRACT

Increasing the linearity of power amplifiers has been an important area of research because its signal integrity influences the performance of the entire transreceiver system and there are strict regulatory requirements on them. Due to the nonlinear behaviour of power amplifiers, third order intermodulation products are generated close to the desired signals and cannot be removed by filters. Increasing linearity will help bring these distortion products closer to the noise floor. However, it is not an easy task to increase linearity without trading off output power. To maintain the same level of output power generated but with higher linearity, many techniques, each with its own pros and cons, have been implemented to linearize an amplifier. Techniques involving feedback are seriously limited in terms of modulation bandwidth whereas methods such as predistortion and feedforward are very difficult to implement. This project seeks to use a simple method of placing terminations directly to the distributed amplifier (DA), making it a device level linearization technique and can be used in addition to the other system level techniques mentioned earlier. To increase linearity over a broad bandwidth of 0.5 to 3.0 GHz, this work proposes using low impedance terminations (LC traps) at the envelope frequency to the input and output of several distributed amplifiers. This research is novel since this is the first time broadband improvement in linearity has been demonstrated using the LC trap method. Two design iterations were completed (first design iteration has four variants to test the output trap while the second design iteration has three variants to test the input trap). The low impedance terminations are implemented using inductor-capacitor networks that are external to the monolithic microwave integrated circuit (MMIC). Design and layout of the DAs were carried out using Agilent's Advanced Design System (ADS). Results show that placing the traps at the output of the DA does not truly affect the linearity of the device at lower frequencies but provide an improvement of 1.6 dB and 3.4 dB to the third-order output intercept point (OIP3) at 2.5 GHz and 3.0 GHz, respectively. With traps at the input, measurement results at -5 dBm input power,

1.375 V base bias (61 mA total collector current) and 10 MHz two tone spacing show a broadband improvement throughout the band (0.5 GHz to 3.0 GHz) of 3.3 dB to 7.4 dB in OIP3. Furthermore, the OIP3 is increased to 19.2 dB above P_{1dB}. Results show that the improvement in OIP3 comes without lowering gain, return loss or P_{1dB} and without causing any stability problems.

ABSTRAK

Meningkatkan “linearity” bagi penguat kuasa merupakan satu bidang penyelidikan yang penting kerana kualiti isyarat yang diterima boleh mempengaruhi prestasi seluruh sistem. Ciri-ciri tidak linear penguat kuasa menyebabkan produk intermodulasi “order” ketiga dihasilkan berdekatan dengan isyarat yang dikehendaki dan tidak boleh ditapis. Walaubagaimanapun, meningkatkan “linearity” bukanlah satu tugas yang mudah tanpa mengorbankan kuasa “output”. Pelbagai teknik (setiap satu mempunyai kelebihan dan kekurangan tersendiri) telah dilaksanakan untuk meningkatkan “linearity” penguat kuasa tanpa mengurangkan kuasa “output”. Teknik-teknik yang melibatkan “feedback” tidak mempunyai jalur modulasi yang lebar manakala “predistortion” dan “feedforward” sangat susah untuk dilaksanakan. Projek ini menggunakan kaedah yang mudah iaitu meletakkan “termination” terus kepada penguat pengedar (DA). Ini menjadikan teknik ini diklasifikasikan sebagai teknik peringkat komponen dan boleh diguna bersama dengan teknik-teknik peringkat sistem yang telah disebut di atas. Demi meningkatkan “linearity” dari 0.5 hingga 3.0 GHz; tesis ini mencadangkan penggunaan “termination” yang mempunyai impedans rendah (LC trap) pada frekuensi “envelope” di “input” dan “output” beberapa DA. Kajian ini merupakan sesuatu yang baru kerana ini merupakan kali pertama peningkatan “linearity” pada jalur lebar telah dilaksanakan menggunakan teknik “LC trap”. Dua jenis rekaan telah dibina (Rekaan jenis pertama mempunyai empat variasi untuk menguji “trap output” manakala rekaan jenis kedua mempunyai tiga variasi untuk menguji “trap input”). “Termination” impedans rendah telah dibina menggunakan rangkaian inductor-kapasitor yang berada di luar litar bersepadu gelombang mikro monolitik (MMIC). Rekaan dan susunan bagi DA telah dibuat menggunakan Advanced Design System (ADS) daripada Agilent. Kajian menunjukkan bahawa meletakkan LC trap di “output” DA tidak mempengaruhi “linearity” DA pada frekuensi rendah tetapi memberi peningkatan sebanyak 1.6 dB pada 2.5 GHz dan 3.4 dB pada 3.0 GHz kepada “third-order output intercept point” (OIP3). Kajian juga

menunjukkan bahawa LC trap di “input” dan pada kuasa -5 dBm, 1.375 V pada voltan “base bias” dan jarak antara dua isyarat sebanyak 10 MHz memberi peningkatan 3.3 dB hingga 7.4 dB dari 0.5 GHz hingga 3.0 GHz. Malahan OIP3 telah ditingkatkan sehingga mencapai 19.2 dB melebihi P_{1dB}. Pencapaian ini merupakan sesuatu yang baru kerana ini merupakan kali pertama peningkatan kepada “linearity” pada jalur yang lebar telah dilaporkan dengan penggunaan LC trap. Data juga menunjukkan bahawa peningkatan kepada OIP3 tidak menjejaskan “gain”, “return loss” dan P_{1dB} serta tidak menjejaskan kestabilan penguat kuasa.

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LIST OF ABBREVIATIONS

ACPR	Adjacent Channel Power Ratio
A/D	Analogue to Digital
ADS	Advanced Design System
AlGaAs	Aluminium Gallium Arsenide
AM	Amplitude Modulation
BJT	Bipolar Junction Transistor
CAD	Computer Aided Design
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CPW	Coplanar Waveguide
DA	Distributed Amplifier
DC	Direct Current
FET	Field Effect Transistor
GaAs	Gallium Arsenide
GSM	Global System for Mobile communications
HBT	Heterojunction Bipolar Transistor
IC	Integrated Circuit
IM3	Third Order Intermodulation
InP	Indium Phosphide
InGaP	Indium Gallium Phosphide
LC Trap	Inductor-Capacitor Network
LNA	Low Noise Amplifier
MESFET	Metal Semiconductor Field Effect Transistor
MMIC	Monolithic Microwave Integrated Circuit
IIP3	Third Order Input Intercept Point
OIP3	Third Order Output Intercept Point
PA	Power Amplifier
PAE	Power Added Efficiency
pHEMT	Pseudomorphic High Electron Mobility Transistor

PM	Phase Modulation
RF	Radio Frequency
Si	Silicon
SiGe	Silicon Germanium
SMT	Surface Mount Technology
VCCS	Voltage Controlled Current Source
VCO	Voltage Controlled Oscillator
WLAN	Wireless Local Area Network

CHAPTER 1
BACKGROUND

1.1 Introduction

There has been a tremendous growth in modern wireless data and voice communication standards over the short span of the last 10 years. Today, mobile and wireless communication systems have turned from a luxury into a necessity and it is nearly impossible to perform day-to-day task without the use of a mobile phone or staying connected on the internet. Advancements in the radio frequency (RF) area have come a long way since James Clerk Maxwell first theorized about electromagnetic waves in 1864.

Many building blocks make up the modern transreceivers we have today. Among them are low-noise amplifiers, mixers, oscillators, filters and power amplifiers [1]. The power amplifier (PA) is one of the most critical components in a transreceiver. The signal integrity of this element influences the performance of the entire system, thus placing strict regulatory requirements on its linearity [2]. According to IS-98 specifications [3], the CDMA power amplifier for the handset is required to transmit up to 28 dBm average power with the Adjacent Channel Power Ratio (ACPR) below -42 dBc (at 885 kHz offset referred to as ACPR1) and -54 dBc (at 1.98 MHz offset referred to ACPR2). Increasing linearity is a major concern because third order intermodulation (IM3) products create distortion to the desired signals in the band of interest and are too close to be filtered. Other specifications for a PA are gain, P_{1dB}, return loss, stability factor and noise figure.

The ongoing process of development in wireless communication has brought about many standards. They belong to four main groups which are digital cordless

telephony, wireless data, analog cellular telephony or digital cellular telephony [4]. Currently, the core problem especially in digital cellular telephony is that there is a lack of a common standard. For example, new WCDMA systems defined in Europe differ from those in USA or Japan. Different frequency allocations for preceding standards, diverse needs of users and political constraints give rise to the aforementioned problem. Having so many wireless standards escalates into many undesired issues. Manufacturers have to develop many different devices and systems for base stations and terminals and ultimately, the end-users have to bear the cost.

The future of the RF world is said to be reconfigurable systems which are able support different standards using several approaches. These approaches include switchable systems, systems with reusable components or systems with multifunctional components [5]. Dual or tri-band phones are not included as reconfigurable systems because they support similar standards in adjacent frequency bands. However, having a reconfigurable system is easier said than done. One main problem is devising design architectures that are able to achieve high linearity over a broad bandwidth [5].

There are several important contributions from this project. Firstly, the LC trap method has been proven successful in improving the linearity over a broadband. In previous work, both the second harmonic and envelope frequencies were shorted out by the traps. However, this project modifies the method for broadband usage by tuning only the envelope frequency since changing the second harmonic frequencies will affect the in-band response of the amplifier.

This project has also compared the effects of adding the traps at either the input or the output of the DA. Placing traps at the input results in an improvement of up to 3.9 dB at the higher frequencies (2.5 GHz and 3.0 GHz). Inserting traps at the input of the DA results in a linearity improvement of up to 7.4 dB throughout the measured band of 0.5 GHz to 3.0 GHz. Furthermore, the OIP3 is reported to achieve up to 19.2 dB above P_{1dB}. These linearity improvements are significant because the other characteristics such as P_{1dB} and in-band S-parameters (gain and return loss) are not lowered. By varying the values of the LC trap, this project has also shown that the

optimum trap values are those providing a small capacitive reactance at the envelope frequency.

1.2 Problem statement

Linearization itself is not an easy task to perform as it involves increasing the linearity by maintaining the output power. Output power generated by the power amplifier can always be traded off for linearity but this is undesirable as it reduces the efficiency of the amplifier. Furthermore, manufacturers are always competing to produce power amplifiers that can achieve higher linearity with higher output power as well.

Many different techniques have been implemented for linearization purposes which include feedback, predistortion and feedforward. Since these methods are applied for the entire transreceiver system, they are known as system level techniques. Each of these techniques has its own pros and cons. Though in general the feedback method provides high levels of linearization, it only works for a very small bandwidth. Predistortion applies to a wide bandwidth but lacks the correction precision found in feedback loops. On the other hand, feedforward combines the best of both these techniques by having good levels of correction and large bandwidth. However, it is very complex and costly to implement.

To date, there has been some work in the area of broadband linearization. Feedforward linearization [6] and self-adaptive bias network [7] techniques have been applied to a distributed amplifier. A programmable predistortion circuit has achieved broadband linearity improvement to a power amplifier [8]. However, no broadband improvement in linearity has been reported with the use of low-impedance terminations, thus making this project novel. Linearity improvements with this technique have only been reported in a narrowband environment using 900 MHz BiCMOS, 2 GHz BiCMOS, 2 GHz Si BJT, 0.88 GHz SiGe BiCMOS, 1.96 GHz SiGe BiCMOS and 1.8 GHz BJT LNAs [9]-[13].

Therefore, this project takes the LC trap method (which is originally a narrowband linearization technique) and applies it over a broadband. By making the low impedance terminations to short out only the envelope frequencies and not the second harmonic, this method can be applied over a broad bandwidth since it does not affect the in-band response of the amplifier. The LC trap method provides moderate amounts of linearization when compared to feedback or feedforward techniques but its greatest quality is that is it very simple method to implement without incurring much in production costs. Furthermore, this method is applied at the device (device level technique) and can be used in conjunction with other system-level linearization techniques mentioned earlier. In the bigger picture, it is a step in the direction of reconfigurable systems by setting out to improve the broadband linearity of a single component (distributed amplifier).

1.3 Objectives

- Design and layout using Advanced Design System (ADS) a 0.5 GHz to 2.5 GHz Distributed Amplifier (DA). The DA must have a minimum gain of 10 dB and a minimum P_{1dB} of 17 dBm (~50 mW). The input and output return loss must be maintained at 10 dB or better. Design rule checks (DRC) and Layout Versus Schematic checks (LVS) must be performed to ensure no error occurs during fabrication of the Monolithic Microwave Integrated Circuit (MMIC).

- Design testboards (sometimes known as Prototype boards) using AutoCAD to allow measurement data to be collected. Testboards must also accommodate external tuning elements to the MMIC.

- Prepare the MMIC for measurement purposes. This includes die attaching and wire-bonding the MMIC to the testboard as well as soldering external surface mount technology (SMT) components and SMA connectors.

- Attempt to improve the linearity, indicated by third order output intercept point, (OIP3) of the DA over the bandwidth of 0.5 GHz to 3.0 GHz by implementing the

low impedance termination at envelope frequency to the input or the output of the DA.

- Analyze the HBT model for third order intermodulation to determine the optimum impedance that must be presented to the HBT for maximum improvement in linearity.

- Collect measurement data which includes S-parameters, P_{1dB} and OIP3 with and without the low-impedance termination while varying parameters such as the termination's inductance and capacitance, base bias voltage and frequency spacing ($f_{spacing}$) of the two input tones.

1.4 Research scope

- The design and implementation of the DA is done using the WIN Semiconductor Corporation's H02U-41 and H02U-43 GaAs HBT foundry process. It is a 2 μm HBT process designed for GSM PA with stringent ruggedness requirements. The process has a f_t = 31 GHz, f_{max} = 110 GHz, I_{DC} current gain, β = 75 and breakdown voltages BV_{CEO} = 17 V, BV_{BEO} = 7 V, BV_{CBO} = 30 V.

- This process also allows a maximum thin film resistor = 50 ohm/sq, capacitor = 600 pf/mm^2 for metal-insulator-metal (MIM) and = 900 pf/mm^2 for stack types.

- The linearity measurements will not be considered for strong nonlinearities sources. Therefore, linearity measurements are made with the DA operating backed off in the linear region and not when it is saturated. This excludes any AM-AM or AM-PM measurements.

- The simplified HBT model used for third order intermodulation analysis includes only the nonlinearities of g_m, r_π, C_{be} and $C_{bc.}$ There are many more nonlinear components in an HBT but these are sufficient to represent the main nonlinearities.

1.5 Thesis Organization

Chapter 1 of this thesis presents an overview of the work completed in this project. It includes the objectives and research scope of which is focused on linearizing the HBT DA over a broadband.

Chapter 2 is the literature review and it is focused on power amplifiers and its characteristics. There are also sections about HBTs and its theory of operation. Furthermore, a comparison of semiconductor materials indicates the advantages of using the InGaP/GaAs HBT. The various types of broadband amplifiers and the reason for choosing the distributed amplifier are also shown. The operation of a distributed amplifier is explained in detail. Since amplifiers are nonlinear devices, the phenomena of nonlinearity and its detrimental effects are presented in this chapter as well. In addition, a description and comparison of other common method of linearization which includes predistortion and feedback techniques are presented.

Chapter 3 starts off by showing the design methodology for the first and second design iteration of the DAs as well as the testboards. Schematics and layouts of the MMIC die performed with ADS and the AutoCAD diagrams of the testboards are shown. This chapter also shows how the linearization technique is applied to the DAs. It involves placing a low impedance termination at either the input or output of the MMIC die. Steps for preparing the MMIC for measurements purposes such as wire-bonding and testboard population are also described. It also has the analysis relating input and output envelope terminations to the improvement in linearity for an HBT. In addition, the simulation, measurement and verification setup are also shown.

Chapter 4 presents the simulation and measurement results for the first design iteration DAs which include traps at the output are presented. These results have been accepted for publication at the International Conference on Intelligent and Advanced Systems, (ICIAS) in Kuala Lumpur [14]. The results for the second design iteration DAs which have traps at the input of the DA are also described. These results have been accepted for publication at the European Microwave Conference (EuMC) in Paris [15].

Chapter 5 concludes the work in this project, describes its contributions and introduces future work that can be carried out. The appendixes include the HBT VBIC large signal transistor model from WIN Semiconductor, the MATLAB coding used in this project and the results from the stability analysis of the DAs.

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

This chapter begins by describing about the power amplifier and common parameters that define its capabilities. The importance of linearity to the power amplifier is explained in detail. The basic operation and characteristics of an HBT with focus on its heterojunction shall also be presented. A comparison of InGaP/GaAs with other semiconductor materials shows the reasons behind choosing this material over the rest. This chapter also includes an examination on the different types of broadband amplifiers and the operational theory of a distributed amplifier. Furthermore, nonlinearity in RF communication systems and its effects are also explained. This chapter also includes a review and comparison of linearization techniques, leading to the motivation of using the LC trap in a broadband environment.

2.2 Background of Power Amplifier

The power amplifier is usually the final active device before the antenna in a wireless transmitter. The function of a power amplifier is rather simple which is to amplify the output signal before transmission. Nevertheless, due to the large amplitude of signals that pass through it, the power amplifier is considered a critical component of the transreceiver and the signal integrity of the PA significantly influences the performance of the entire system. The signal integrity (quality) is determined by the linearity of the PA, making this property extremely important and must be maintained above a specified level. For example, the CDMA power amplifier for the handset is

required to transmit up to 28 dBm average power with the Adjacent Channel Power Ratio (ACPR) below -42 dBc (at 885 kHz offset referred to as ACPR1) and -54 dBc (at 1.98 MHz offset referred to ACPR2) [3].

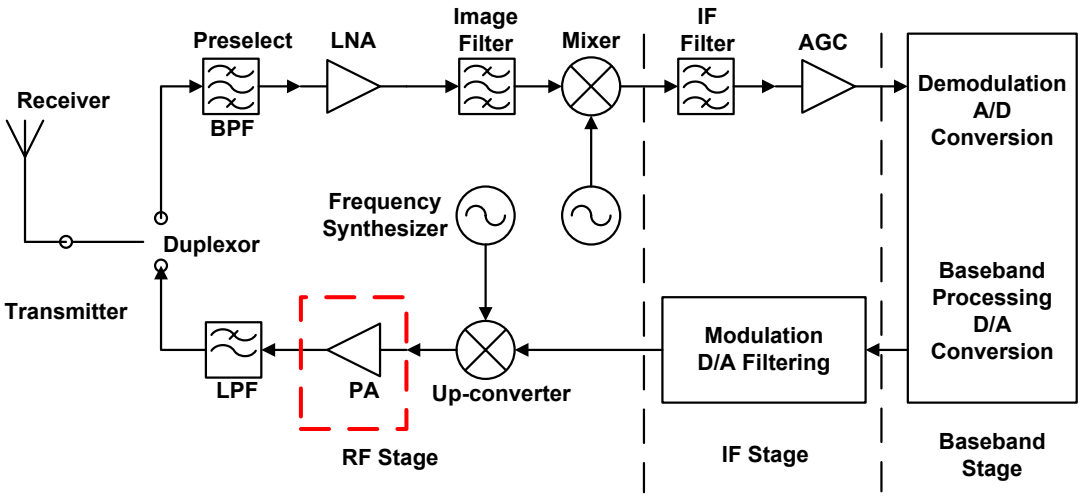

Figure 2.1: RF transreceiver architecture

Fig. 2.1 is a typical RF transreceiver architecture where the PA is highlighted in red. Today, many commercial or military wireless standards co-exist in the frequency spectrum and the most often used frequency range for a wireless transreceiver is from 400 MHz to 6 GHz [4]. In commercial applications, there currently exist needs to switch from one application to another within one portable device. A wideband transreceiver is often desired inside intelligent front-ends in military applications. As a result, configurable RF systems which can be tuned into different frequency bands have generated great interest recently [5], [16]. Popular transistors used in power amplifier designs in portable transreceivers are MESFETs, pHEMTs and HBTs. For power amplifiers with more than 20 dBm output power, the CMOS technology was deemed not suitable due to its low output power generation and higher substrate loss.

2.3 Characteristics of Power Amplifier

The main requirement of a power amplifier is the ability to deliver power up to a specified level. This requirement can be quantified by evaluating the output power with a single tone source. A power amplifier is usually defined by its output power with its gain compressed by 1 dB (P_{1dB}). P_{1dB} is an indication of the maximum output power that can be achieved before gain compression. The P_{1dB} shown in Fig. 2.2 is about 16 dB.

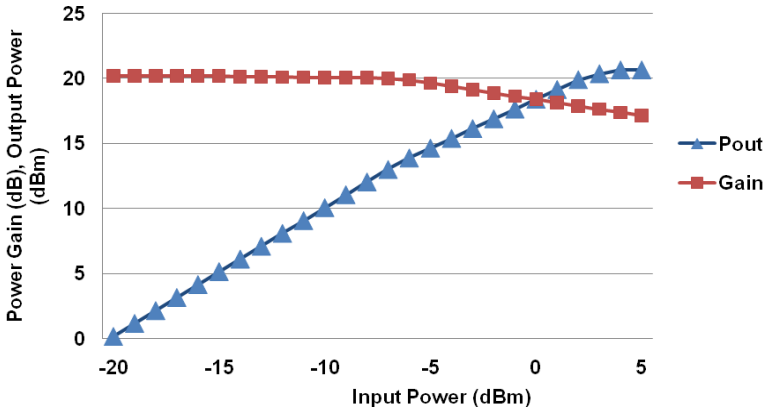

Figure 2.2: Power amplifier performances under one tone test

Another parameter important to power amplifiers is the Power Added Efficiency (PAE). PAE is given by

$$PAE = \left(\frac{P_{outRF} - P_{inRF}}{P_{DC}} \right) * 100 \qquad (2.1)$$

PAE is similar to drain efficiency for FET devices but it takes into account the RF power added to the input of the device, making it a more accurate measure of efficiency. Efficiency quantifies effectiveness of the conversion of DC power to RF power and this has direct impact on battery life and talk time in portable systems.

Another measurement requiring a single tone source is the AM-AM (gain) and AM-PM (phase) distortion curve. Since the output power is related to the input by the relation

$$P_{out}(P_{in}) = P_{in}.G(P_{in})e^{j2\pi\psi(P_{in})} \tag{2.2}$$

As shown in (2.2), the input power is dependent on both gain (*G(Pin)*) and phase (ψ*(Pin)*) and plays an important role in determining linearity characteristics. However, the value of AM-PM is very small, making it a difficult parameter to measure accurately. Phase changes in the fundamental signal introduced by AM-PM distortion depends on signal amplitude. As a result, a large change in amplitude is needed before a visible effect on phase can be recorded. The similar observation is made for AM-AM distortion. Using amplitude conversions as a figure of merit for nonlinearity is a problem because they measure nonlinearity on the basis of the fundamental signal (which comprises of a strong linear term). Since nonlinear effects in the fundamental are small, the measurement of AM-AM and AM-PM is highly sensitive to measurement errors. The AM-AM and AM-PM distortion curves are shown in Fig. 2.3.

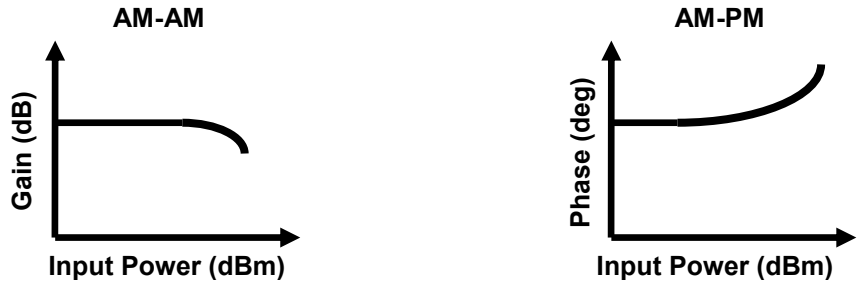

Figure 2.3: AM-AM and AM-PM distortion

A two-tone test becomes the standard assessment of the distortion characteristics of an amplifier. Two input signals spaced closely in terms of frequency become the input into the amplifier, which generate new output signals in the frequency spectrum. Fig. 2.4 shows the second order and third order intermodulation product as a function of output power. The intercept point between fundamental signal and third harmonic is defined as third order intercept point (IP3).

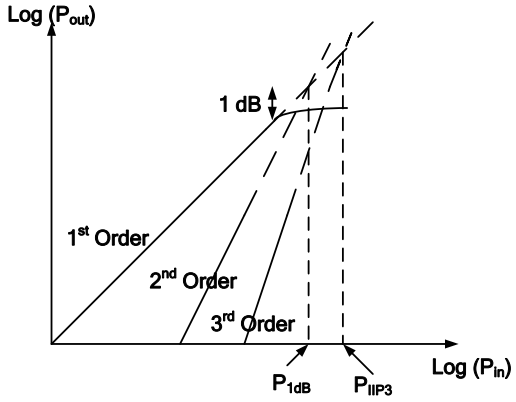

Figure 2.4: Second and third order intermodulation in two tone test

Intercept point represents the intersection between the extrapolated 1:1 slope of fundamental gain, and the 3:1 slope of the third order IM products. The IP concept can be best explained using a proof relating the IP3 and the 1 dB compression point, P_{1dB} [17]. This proof assumes that the power series can be approximated to include terms only up to the third degree. Firstly, this proof considers an amplifier driven with a sinusoidal signal that causes a gain compression of 1 dB. If this signal amplitude, measured at the input, is V_{ic}, the fundamental output voltage is given as

$$V_{oc} = a_1 V_{ic} \cos \omega t + a_2 {V_{ic}}^2 \cos^2 \omega t + a_3 {V_{ic}}^3 \cos^3 \omega t \tag{2.3}$$

From the trigonometric identity,

$$\cos^3 \theta = \frac{1}{4}\left(3\cos\theta + \cos 3\theta\right) \tag{2.4}$$

the output voltage amplitude at the fundamental frequency is

$$V_{oc} = a_1 V_{ic} + \frac{3}{4} a_3 {V_{ic}}^3 \tag{2.5}$$

When there is no compression or nonlinear terms, the output voltage amplitude would be $a_1 V_{ic}$. If that is reduced in power by a factor of 1 dB, the output voltage becomes

$$V_{oc} = a_1 V_{ic} 10^{-0.05} \tag{2.6}$$

Combining the (2.5) and (2.6) gives

$$a_1 V_{ic} 10^{-0.05} = a_1 V_{ic} + \frac{3}{4} a_3 {V_{ic}}^3 \tag{2.7}$$

From (2.7), the sign of a_3 must be negative for gain compression to occur. A negative sign is introduced for a_3 and (2.7) is rearranged to give

$${V_{ic}}^2 = \frac{4a_1\left(1-10^{-0.05}\right)}{3a_3} \tag{2.8}$$

Equation (2.8) gives a value for the input amplitude of a sinusoidal signal that causes 1 dB gain compression, in terms of the two power series coefficients, a_1 and a_3. Now we consider the same amplifier, having the same bias and tuning conditions but with two-tone signal applied to its input and both signals having equal amplitude. The amplitude of each carrier V_{ip3}, at the IP3 will be given by

$$a_1 V_{ip3} = \frac{3}{4} a_3 {V_{ip}}^3 \tag{2.9}$$

Rearranging the (2.9) gives a relation between the input third-order intercept signal amplitude and the two power series coefficients

$${V_{ip3}}^2 = \frac{4a_1}{3a_3} \tag{2.10}$$

Combining (2.8) and (2.10) gives

$$\left(\frac{V_{ip3}}{V_{ic}}\right)^2 = \frac{1}{1-10^{-0.05}} \tag{2.11}$$

This gives to a ratio of 9.2 or about 9.6 dB. So the IP3 is about 10 dB higher than the P_{1dB}.

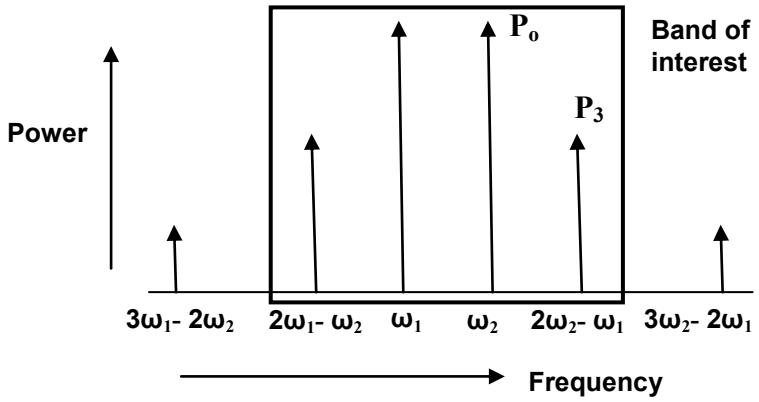

Figure 2.5: Two tone intermodulation spectrum

From the output spectrum, linearity is measured by obtaining the third order output intercept point (OIP3) as shown in Fig. 2.5. Equation (2.12) expresses the OIP3 in terms of power of the fundamental tone, P_o and power of the third order products, P_3. When OIP3 increases, the difference between P_o and P_3 increases as well and the third order products approach the noise floor. Thus, when third order products get smaller, the linearity increases.

$$OIP3 = P_o + \left(\frac{P_o + P_3}{2} \right) \tag{2.12}$$

The linearity for amplifiers especially LNAs are sometimes stated as the Third Order Input Intercept Point (IIP3). The IIP3 = OIP3 – Transducer Power Gain.

Nonlinearity characterization using two-tone analysis is very useful for characterizing amplifiers in the weakly nonlinear region. In the strongly nonlinear region, higher order IMD products (such as fifth or seventh order) become much more significant because the amplifier is driven further into compression. The cause for this situation is due to the limiting behaviour of the transistors. The presence of multiple strong IMD products in this region requires a different method of characterizing nonlinearity for PA design.

Adjacent channel power ratio (ACPR) is defined as the measured power in an adjacent communications channel of a specified bandwidth relative to the power in the main channel of specified bandwidth, shown in Fig. 2.6.

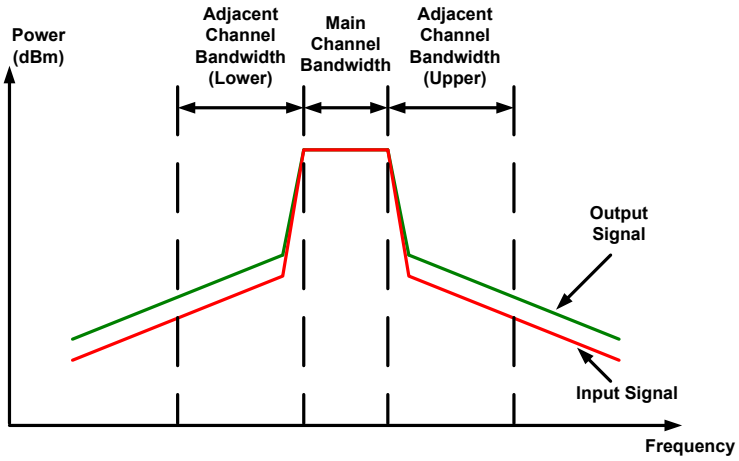

Figure 2.6: Adjacent Channel Power Ratio

An analog example could be two frequency modulated (FM) signals in adjacent channels of a multicarrier transmitter. These FM signals would exhibit modulation sidebands around the carrier, causing the IMD products to exhibit sidebands as well. ACPR is basically a measure of power in the sidebands due to all of the IMD products relative to the desired channel. With lower ACPR, the channels can be packed tighter in a given amount of bandwidth with minimal interference to one another.

2.4 Heterojunction Bipolar Transistors

Transistors are semiconductor devices with three, or more terminals. Transistors are considered a breakthrough in the electronics world because its third terminal enables output current to be controlled by a relatively small and low-power input signal. This means that transistors in amplifiers can be used to achieve current gain, voltage gain or power gain.

A bipolar transistor has semiconductor regions called the collector (C), base (B) and emitter (E). An npn BJT has n-type semiconductor at the emitter and collector

and the p-type semiconductor at the base. The positive sense of current flow in this transistor is from the collector, through the base and to the emitter. The collector current is dependent on the number of carriers injected into the base region from the base terminal. When fabricated using silicon, a bipolar transistor is called a bipolar junction transistor (BJT), while in a compound semiconductor technology, it is called a heterojunction bipolar transistor (HBT). A typical HBT structure is shown in Fig. 2.7.

Since the beginning of the 1980s, heterojunction bipolar transistors (HBT) have made rapid progress in maturity and can be found in a wide variety of applications. HBTs can be found in microwave high power and high efficiency amplifiers for radar and communication systems, microwave integrated circuits (IC) for portable communication, broadband analog ICs such as feedback amplifiers, logamps, and voltage control oscillators (VCO) as well as A/D converters for communication and instrumentation [18].

There are several reasons in choosing HBT over other transistor types. Firstly, compared to FET technologies, bipolar transistors offer higher collector efficiency due to a lower knee voltage, higher breakdown and exponential transconductance [19]. HBT technology has also shown the highest IP3 to DC power figure of merit. Although HBT devices have a nonlinear transconductance, the device nonlinear base-emitter capacitance can be used to cancel intermodulation distortion products. MMIC HBT power amplifiers have been reported with peak OIP3 of 34 dBm and IP3/P_{DC} power ratio of 21:1 [20]. In terms of power delivered per unit area, HBTs have high power density which can be attributed to the high transconductance and low parasitic device resistances. A HBT consume only 60% of the area of a silicon bipolar transistor and only 20% of the area of a GaAs MESFET for an equivalent output power requirement [19]. Currently, there are three types of HBT technology that are commercially available which are Si/SiGe, GaAs and InP based HBTs [21]. The InGaP/GaAs HBT has been chosen for this project (InGaP forms the emitter layer and GaAs forms the base layer for the HBT).

With higher current density and higher breakdown voltage, HBTs have been reported in power amplifiers up to 9.9 W output power at the X band [22]. HBTs have 5 – 10 dB higher device power gain compared to regular bipolars, making them achieve higher power-added efficiency (PAE). 68% PAE has been attained with GaAs HBTs at X-band, along with high gain and high power density [23]. Even though AlGaAs has been the dominant wideband gap material for the emitter, InGaP provides a larger valence band discontinuity to suppress hole current, resulting in a significant increase in the current gain. Therefore, the InGaP/GaAs HBT technology has been chosen since it is the right choice for the implementation of a broadband, high power and high linearity amplifier.

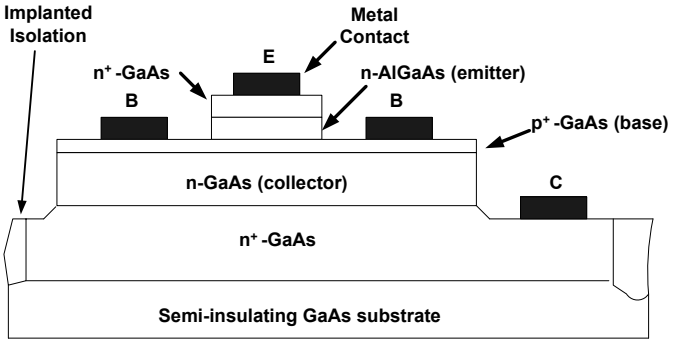

Figure 2.7: Typical HBT structure

2.4.1 Heterojunction

Although HBTs were invented and patented in the 1948 by W. Shockley [24] and investigated by H. Kroemer in the 1957 [25], the HBT technology did not become available until the 1980s. The basic principle of current gain in the bipolar transistor originates from the injection efficiency of the emitter-base junction. For an npn transistor, this would be the ratio of electron current to hole current, I_n/I_p. A HBT incorporates a heterojunction at the base-emitter junction, with a larger bandgap in the emitter [26]-[27]. Base acceptor doping, N_A, emitter donor doping, N_D, and the current gain, β, in traditional homojunction BJTs are defined by

$$\beta \approx \frac{D_n N_D W_E}{D_p N_A W_B} \tag{2.13}$$

where W_B and W_E is the thickness of the base and emitter region and D_n and D_p is the diffusivity for a n-type and p-type semiconductor respectively.

By substituting a wider bandgap material in the emitter (such as AlGaAs or InGaP), there is significant discontinuity in both conduction and valence bands. Energy of the valence band discontinuity presents a barrier to the holes. This barrier suppresses significant amount of hole diffusion into the emitter (i.e. base current) and enhances the injection of electrons into the base, thereby increasing injection efficiency and leading to a higher current gain. The device current gain in the presence of a heterojunction is modified to

$$\beta \approx \frac{D_n N_D W_E}{D_p N_A W_B} e^{\frac{\Delta E_g}{kT}} \tag{2.14}$$

where ΔE_g is the total energy difference in the discontinuity of the heterojunction.

The successful applications of heterojunctions in various devices are due to the capability of epitaxy technology to grow lattice-matched semiconductor materials on top of one another with virtually no interface traps. A good combination for heterojunction devices is two materials of similar lattice constants but different energy gaps, shown in Fig. 2.8. Examples are are GaAs-based (emitter/base => InGaP/GaAs), InP-based (emitter/base => InP/InGaAs) and Si-based (emitter/base => Si/SiGe).

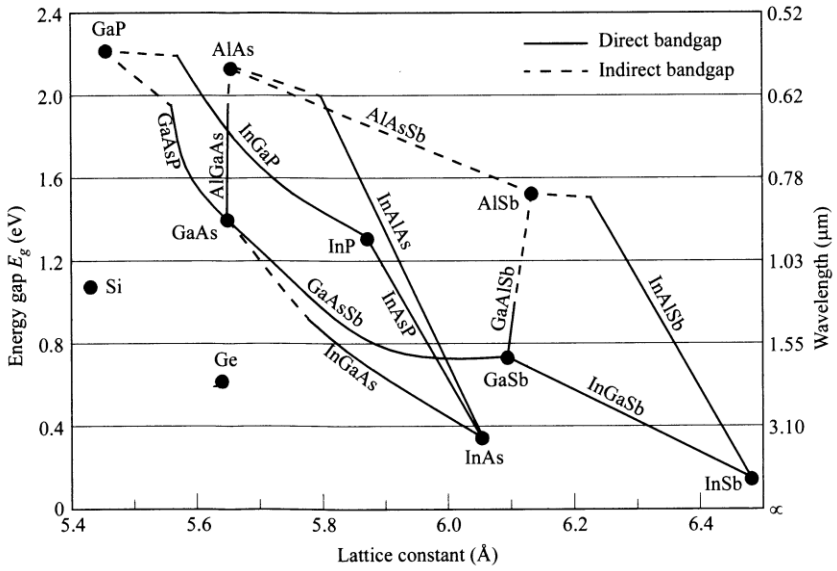

Figure 2.8: Energy gaps versus lattice constant for various materials [15]

Typical doping profile for an HBT is shown in Fig. 2.9 where the base doping is higher than the emitter doping. The high base doping brings many advantages. Firstly, it brings about lower base resistance, improving f_{max} and current crowding. Higher base doping also improves the Early voltage and reduces the Webster effect.

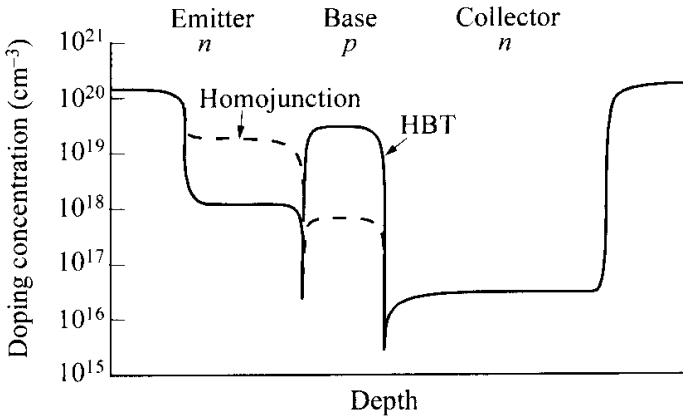

Figure 2.9: Doping profile for HBT [15]

Early voltage is improved due to suppression of the depletion in the base side of the base-collector junction and the elimination of the Webster effect is due to unlikelihood of minority carrier concentration exceeding the acceptor doping [21].

Early effect occurs when there is a lack of saturation in the common-emitter characteristics following a large increase in β with V_{CE}. The voltage at which the extrapolated output curves meet is called the Early voltage. High injection occurring when the minority carrier density in the base is equal or larger than the base doping density is known as the Webster effect.

The band discontinuity also allows the reduction in emitter doping, which results in a lower base-emitter capacitance C_{BE}, while maintaining high current gain. Furthermore, larger emitter bandgap will provide a larger built-in potential.

Base transit time is a strong function of the base width [28]. Since the Early effect has been significantly suppressed with highly doped base, it is possible to decrease base width to significantly improve the base transit time, thereby increasing f_t. However, there is a trade off in the decrease of the base width since the base resistance, R_B is inversely proportional to W_B given by

$$R_B = \frac{\rho_B s_B}{l_E W_B} \tag{2.15}$$

R_B and C_{BC} is related to the maximum oscillation frequency f_{max} by the relationship

$$f_{\max} = \sqrt{\frac{f_t}{8\pi R_B C_{BC}}} \tag{2.16}$$

This makes the base width of an HBT a very important design parameter to optimize the f_t and f_{max} of the device. Due to a very narrow base of GaAs HBTs, the collector transit time becomes the dominant delay component in normal operating conditions [29].

2.4.2 Comparison of InGaP/GaAs with other Semiconductor Materials

Fig. 2.10 indicates a comparison between the transit frequency, f_t and the collector-emitter breakdown voltage, BV_{CEO} for commercially available HBT technologies. The f_t is usually increased by scaling down devices and decreasing the breakdown voltage. From Fig. 2.10, the advantage of III-V materials over Si is not in reaching higher frequencies, but in improved power-handling capabilities. This is enabled by higher breakdown voltage and larger maximum currents.

III-V (such as GaAs, InP) HBTs are suitable for analog applications since they combine high transconductance with high output resistance, high breakdown voltage, low turn-on nonuniformity and low 1/f noise [30]-[32]. The III-V HBT technology has an advantage over Si and SiGe in terms of $f_t - BV_{CEO}$ breakdown product. Comparing Si and GaAs materials, the smaller silicon bandgap causes the device to avalanche breakdown at a lower voltage. So although advanced silicon technologies have achieved more than 100 GHz in f_t, they are still limited by a low BV_{CEO} of 2 V. The f_t for GaAs HBTs at a given breakdown voltage is almost triple compared to Si [30]. This translates to better bandwidth for a broadband amplifier since f_t relates to the gain-bandwidth product. A Darlington feedback amplifier with 8 dB gain from DC to 30 GHz has been reported [33]. A DHBT MMIC power amplifier with P_{1dB} of 13.5 dBm at 94.5 GHz has been successfully implemented [34].

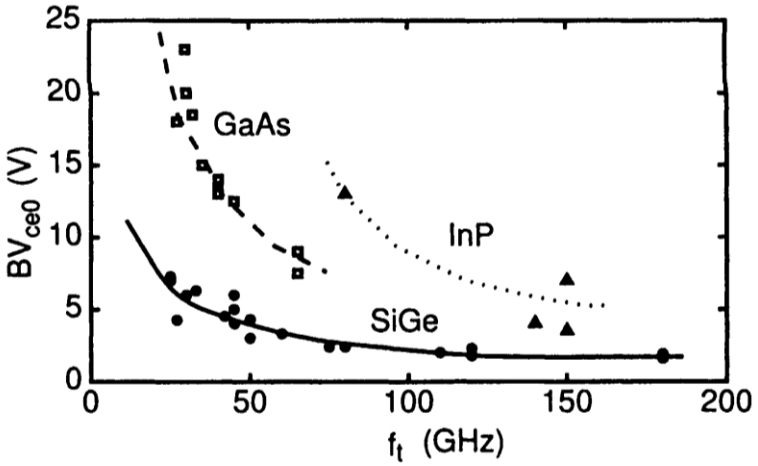

Figure 2.10: CE breakdown voltage versus f_t for common HBT technologies [21]

SiGe technology is advantageous if integration with CMOS digital circuitry is necessary. They offer lower costs in mass production, compared to the III-V based HBTs. On the other hand, the initial development costs such as photolithographic masks are much higher in the case of Si technology compared to the III-V technologies. Hence, special circuits in low volume production may even be cheaper on GaAs or InP than on Si.

Even though the abundance of silicon makes it cheaper to adopt, many properties of GaAs makes it the better choice for mobile phones, satellite communications and radar systems [35]. These include higher saturated electron velocity and higher electron mobility. GaAs also generate less noise then silicon devices when operated at high frequencies and has a lower substrate loss compared to silicon.

Minority carrier mobility and electron drift velocity are important material properties because they affect the intrinsic delay (consisting of the base and collector transit times). Minority carrier (electron) mobility as a function of acceptor impurity is shown in Fig. 2.11 for GaAs and Si at room temperature. It is evident that GaAs has much higher minority carrier mobility over a wide range of acceptor doping.

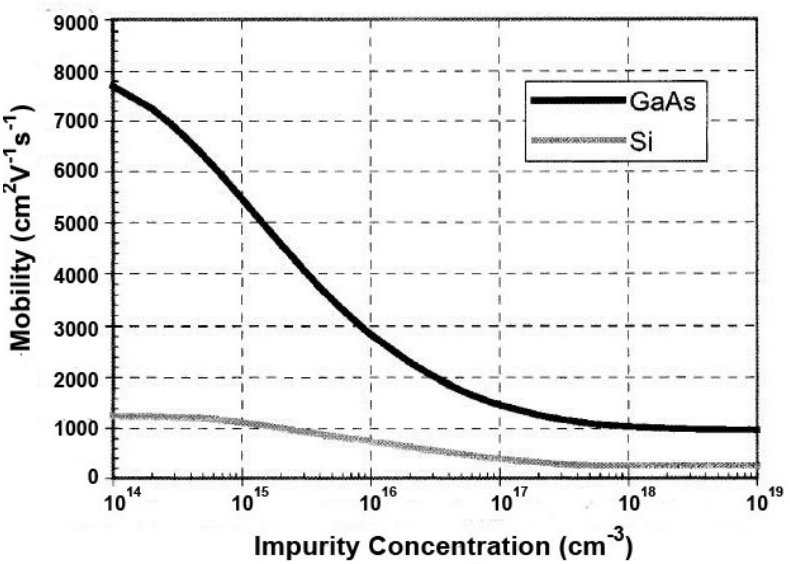

Figure 2.11: Minority carrier (electron) mobility as a function of impurity concentration at T = 300 K [36]

The minority carrier mobility is most relevant in the base transport of the bipolar transistor where the base transit time is controlled by the relationship

$$\tau_B = \frac{W_B^{\,2}}{2D_n} \tag{2.17}$$

W_B is the thickness of the quasi-neutral base region and D_n is the electron diffusivity, related to mobility by Einstein's relationship,

$$D_n = \mu_n\left(\frac{kT}{q}\right) \tag{2.18}$$

Therefore, higher minority carrier mobility generally results in lower base transit time, where base transit time is related to the f_t of the device via the total delay.

$$\frac{1}{2\pi f_t} = \tau_{EC} = \tau_{RC} + \tau_{gm} + \tau_B + \tau_C \tag{2.19}$$

The field dependence of the electron drift velocity is shown in Fig. 2.12

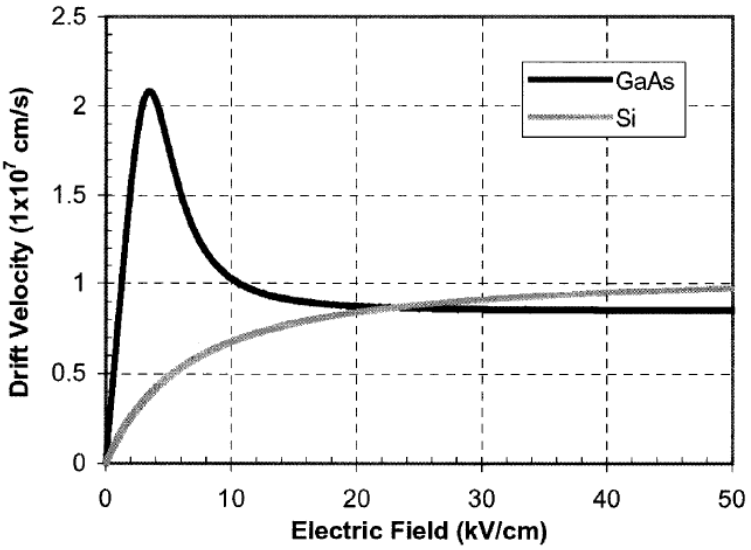

Figure 2.12: Electron drift velocity versus electric field for GaAs and Si [37]

The electron drift velocity is an important material parameter for bipolar transistors because it is one of the key factors of collector transit time, τ_C. Electrons transverse the collector depletion region by the drift mechanism with delay,

$$\tau_C = \frac{W_C}{2v_e} \tag{2.20}$$

where W_C is the collector depletion width and v_e is the electron drift velocity. From Fig. 2.12, when the GaAs collector is biased appropriately in the low electric field region, it is possible to obtain collector transit times that are significantly lower than collectors made of Si.

Although GaAs itself has attractive inherent material properties, it is the ability to form latticed-matched heterojunctions with epitaxial growth techniques such as metalorganic chemical vapour deposition (MOCVD) and molecular beam epitaxy (MBE) that distinguishes GaAs heterojunction based devices from traditional Si devices. As shown in Fig. 2.8, AlGaAs/GaAs and InGaP/GaAs are good examples. It should be noted that InGaP is a wider bandgap semiconductor when lattice matched to GaAs as shown in Fig. 2.13.

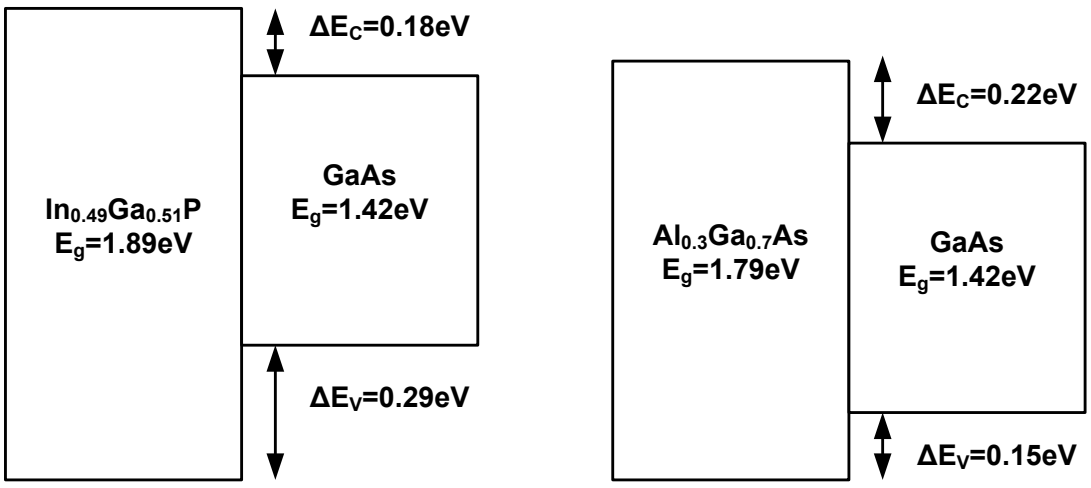

Figure 2.13: Band line up for InGaP/GaAs and AlGaAs/GaAs heterojunctions

AlGaAs has been the predominant wideband gap material for the emitter due to excellent lattice match for a very wide range of Al mole fraction. However, InGaP has recently become a more attractive material for several reasons. Firstly, the band line up of InGaP/GaAs heterojunction is more favourable to the base-emitter design of the HBTs where there is a larger valence band discontinuity to suppress hole current, resulting in a larger increase in the current gain. Other advantages of using InGaP as opposed to AlGaAs for the emitter include selective etching between InGaP and GaAs (process yield improvement) [38], fewer deep-level traps resulting in lower noise figure [39] and longer mean time to failure when operating at high currents [40]-[41].

2.4.3 Operation of HBT Transistors

Commonly, III-V HBTs are npn-transistors, where the two diodes share a thin p region which is the base of the transistor. Four operation conditions exists: (1) the off state, with both pn junctions reversely biased and zero current flowing, (2) saturation, with both pn junctions in forward bias (HBT acts as a short circuit and current flowing is limited by extrinsic resistances), (3) active-forward operation, with one pn junction (base-emitter) in forward bias, and the other one (base-collector) in reverse bias. In this operation condition, the base-emitter current I_b controls the collector-emitter current I_c, resulting in a current gain $\beta_f = I_c/I_b$. The reason is that the majority of the electrons leaving the emitter diffuse through the base into the collector, thereby contributing to I_c. Only a small fraction recombines in the base, yielding I_b. And (4) reverse operation, which is similar to active-forward operation, but with collector and emitter interchanged. Figure 2.14 shows the schematic cross section of an HBT.

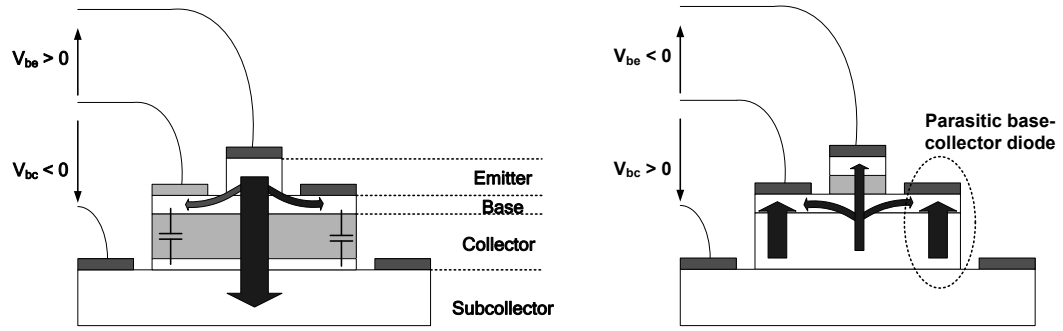

Figure 2.14: Cross section of HBT

2.5 Broadband Amplifiers

W.S. Percival, in 1935, discovered that the gain-bandwidth product is greatly affected by the capacitance and transconductance of the conventional electronic valve. He also discussed about a thermionic valve with one or more electrodes made in the form of a spiral coil. The coil and electrode capacitance form a distributed transmission system thus leading to the idea of distributed amplification [42]. The potential of Percival's work was not fully appreciated until his idea was investigated by Ginzton in 1948 [43] and Horton in 1950 [44].

Since then, the developments of distributed amplification techniques have increased rapidly. Between the 1970 and early 1980s, advanced GaAs FETs and MESFET technology were heavily involved in the design of hybrid microwave amplifiers and circuits [45]-[47]. Subsequently, broadband preamplifiers for small signals [48]-[49] and medium power amplifiers for larger signals were developed [50]-[51]. Archer developed a hybrid GaAs FET distributed amplifier that has a gain of 12 dB and noise figure of 3-6 dB over a bandwidth of 0.1 to 6 GHz [52].

Recently, InGaP/GaAs HBTs have been the key technology in delivering solutions for both high efficiency and high linearity MMIC power amplifiers in various wireless communication systems such as GSM, CDMA and WLAN [53]. Although power amplifier modules (PAM) consisting of MMIC power amplifiers,

matching networks and control circuits can meet the demand of power amplification with multi-frequency band coverage [27], this implementation requires multiple MMIC chips, making the biasing circuit very complicated and increases the number of components used. In order to simplify the design of multi-band PAM, alternative circuit topologies to incorporate broadband amplifier designs have been proposed. These include balanced amplifiers, distributed amplifiers and amplifiers with variety of matching networks.

2.5.1 Reactively Matched Amplifier

The reactively matched amplifier uses lossless matching networks, with either lumped or distributed elements. By selectively creating reflections between the matching network and active device, the matching circuits are used to accomplish gain compensation. In practice, by optimizing the input matching circuit, maximum gain can be achieved. Optimizing the output matching circuit can help achieve maximum output power and power added efficiency. The disadvantage of this type of amplifier is its relatively poor impedance match.

Although the lossless matching circuit provide the desired match over a narrow band of frequencies, the matching at other frequencies is degraded. For broad bandwidth, input and output matching must be traded off to maintain flat gain [54]. This can be improved by employing isolators in the case of a single-ended design or hybrid couplers such as combiners and dividers in the case of balanced amplifiers. However, in the single ended case, this will result in extra cost and an increase in overall size of the amplifier module [55]. The balanced amplifier approach results in an increase in output power of 3 dB but comes at the expense of double the DC power consumption and lower gain equal to that of a single ended amplifier.

Nevertheless, if the device is only conditionally stable, the input and output cannot be matched to 50 ohms because of potential instability. Therefore, it is difficult to achieve good input/output match, flat gain together with good stability. Tserng reported the first reactively matched 2 – 18 GHz power amplifier using GaAs

MESFET devices that achieved average PAE of 8% - 15% and output power of 23 dBm [56]. The first reactively matched MMIC multioctave PA operating over 6 – 18 GHz has been introduced by Palmer [57].

2.5.2 Lossy Matched Amplifier

Lossy match technology can compensate the intrinsic gain roll-off of the transistor to acquire flat gain. The most typical topology is to employ resistors in series with high impedance stubs on both the input and output, as shown in Fig 2.15. R_G and R_D are the gate and drain resistances.

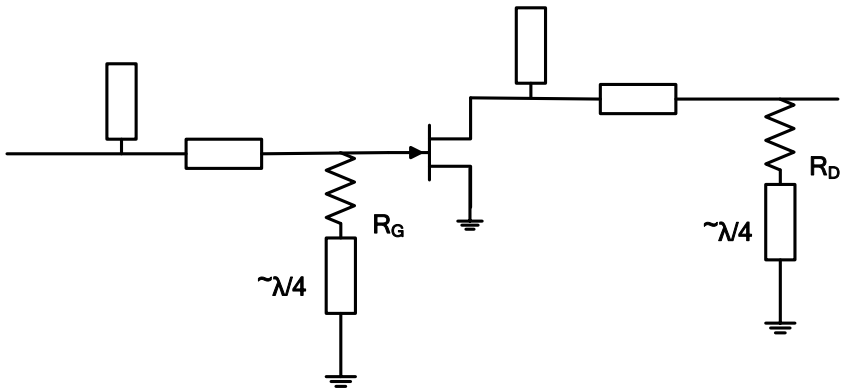

Figure 2.15: Lossy matching

At low frequencies, the stubs have little reactance and the resistors load the transistor and lower its gain. At high frequencies, the stubs have high reactance and the resistors have little effect on the transistor. Hence, the matching network can introduce a positive gain slope to compensate the transistor's gain roll-off without resorting to mismatching [58]. The benefits of this technique are flat gain, good input/output match, low DC power consumption and improved stability of the amplifier. The drawback is lower output power and gain plus degraded noise figure.

2.5.3 Feedback Amplifier

The basis of the feedback technique is that negative feedback is applied to the FET by connecting a resistor from the Drain to the Gate. This stabilizes the device at low frequencies and can make the input and output impedances much closer to 50 ohms, which is beneficial since FETs can have very negative input resistance and high output resistance at low frequencies.

Fig. 2.16 shows the schematic of a matched feedback amplifier suitable for use up to 10 GHz [59]. R_{FB} is the key feedback element and its value determines the basic gain and bandwidth, which have to be traded off against one another. R_{FB} controls the gain level, but at high frequencies the reactance of L_{FB} increases, reducing the amount of negative feedback. Therefore, the effect of L_{FB} is to maintain flat gain and give operation up to a higher frequency.

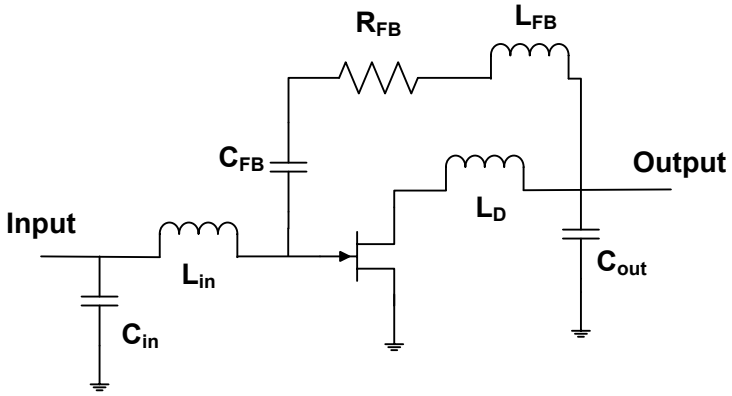

Figure 2.16: Feedback amplifier

L_D is chosen to compensate for the C_{ds} of the FET, providing gain peaking at the upper edge of the frequency response. Typically, low pass matching structures are used at the input and output to achieve broad bandwidth. Matching elements are L_{in}, C_{in} and C_{out}. C_{FB} is a DC block which isolates the positive drain bias from negative gate bias. Bandwidths as high as 1 to 10 GHz and 6 to 18 GHz have been achieved [60]-[61].

There are many advantages for the feedback amplifier. Firstly, the circuit is less complex compared with the reactively matched and travelling wave amplifier circuits. The amplifier can provide higher power-added efficiency performance when compared with the conventional travelling wave amplifiers. Besides that, it provides lower distortion and sensitivity to active device variations. This amplifier also offers a cost-effective multioctave bandwidth amplifier design and has excellent performance in achieving flat gain and unconditional stability.

The main disadvantage of this type of amplifier is the decrease in output power and noise figure over the lower end of the frequency band due to loss associated with the feedback resistor. The amplifiers provide broad bandwidth performance at the expense of low gain, low output power, high noise figure and poor power efficiency, caused by loss in the feedback resistor, used in the feedback network [59].

2.5.4 Balanced Amplifiers

A balanced amplifier shown in Fig 2.17 employs two amplifiers in conjunction with two hybrid 90^o hybrid junctions. An ideal 90^o hybrid splits its input power equally in the forward direction while there is no power coupling to its fourth port. The branched-out signal lags behind the direct path by 90^o. Hence, the power input at port 3 of the first hybrid junction appears at port 1 and port 2 and it is not coupled at all to port 4.

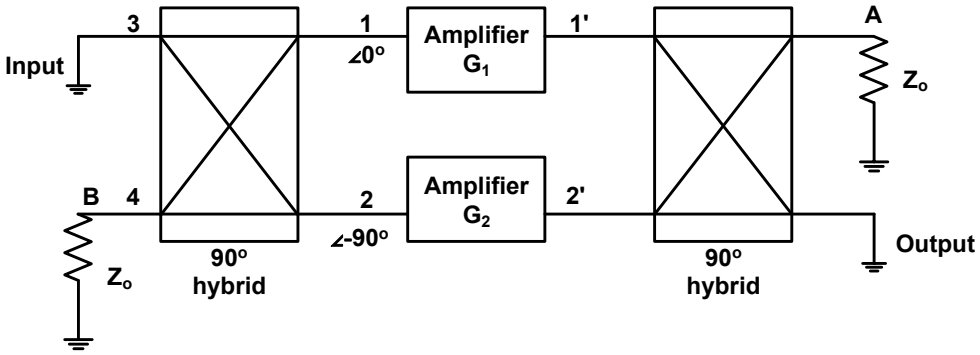

Figure 2.17: Balanced amplifier

The signals fed to amplifiers, G_1 and G_2 have the same magnitudes but a phase difference of 90^o. This causes the signals that are reflected back to have identical magnitudes but a constant phase difference. Entering port 1 and port 2, the reflected signals split with equal powers at port 3 and port 4. Thus, two signals appearing back at port 3 are equal in magnitude but 180^o out of phase with respect to each other and therefore cancel out. Signals appearing at port 4 are in phase and absorbed by the load.

Signals amplified by the two amplifiers are fed to a second hybrid that is matched terminated at port A. Signals entering at its port 1' and port 2' appear at the output while cancelling out at port A. Thus, the overall gain of an ideal balanced amplifier is equal to that of an amplifier connected in one of its channels.

The main advantage of balanced amplifier is high output power, good input-output return loss and easy to be cascaded with other amplifiers [62]. However, the couplers in balanced amplifiers are too big to be used in MMIC technology and needs more DC power consumption and active devices.

2.5.5 Distributed Amplifier

In the early 1980s, distributed amplification became popular since the realization of GaAs MESFETs could be used in a monolithic distributed amplifier to achieve decade bandwidth amplification [63]. With MMIC technology, the distributed amplifier can achieve extraordinary wide bandwidths with a simple circuit topology that is relatively insensitive to process variations.

The DA (or travelling wave amplifier) is associated with two artificial transmission lines, one that makes up the input base line and another that forms the collector output line. The artificial lines basically consist of a network of series inductance and shunt capacitances. The shunt capacitances of the base line are supplied by the C_{be} of the HBTs, whereas the collector line shunt capacitors are

supplied by the HBT's C_{ce}. Lengths of the transmission line and inductors (L_A and L_B) are used to form the series inductances.

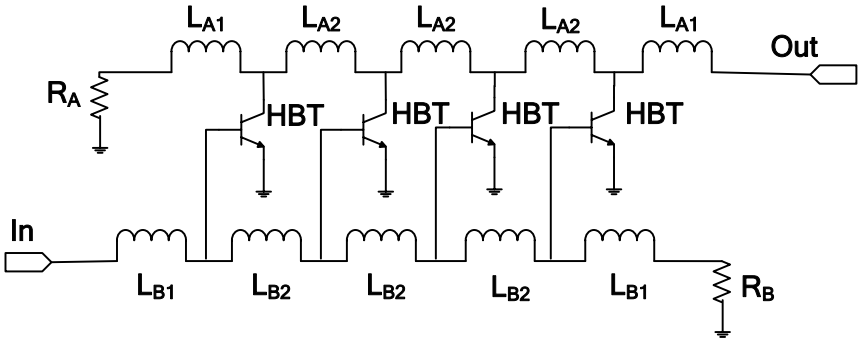

Figure 2.18: Distributed amplifier

Fig. 2.18 shows the circuit diagram of a DA. The problems associated with a broadband match are solved since the input and output capacitances of the active devices are absorbed in the distributed structures [64]. As the input signal travels down the base (input) line, it excites each HBT in turn before being absorbed by a terminating resistor, R_B. The transconductance of the HBT amplifies the signal on the input line and feeds it into the collector (output) line. If the phase velocities in the base line and collector line are roughly equal, then the signals from each HBT will add constructively at the output port. At high frequencies, the signals will largely cancel out at the reverse end of the collector-line, though this is not the case at low frequencies. A collector-line termination, R_A absorbs any undesired signals present at the reverse end. The resulting amplifier exhibits low sensitivities in process variations when realized in MMIC technology and is relatively easy to design and simulate [64].

The first 1 - 13 GHz monolithic travelling wave amplifier was presented by Ayasli in 1982 [65]. He also reported 2 - 20 GHz decade band amplification with 30 dB gain with GaAs FETs in monolithic form [64]. Kim and Tserng [66] described a novel concept of reducing the gate line losses by using series capacitors with the GaAs MESFET devices. An output power of 0.5 W was achieved with 4 dB small signal gain over 2 – 21 GHz bandwidth.

The major application of this type of amplifier has been in electronic warfare, radar and broadband communication systems as well as measurement instrumentation. The main advantages of this amplifier are its very wide bandwidth and circuit stability characteristics. Isolation from output to input is good and its non-resonant nature of the input and output impedance results in a stable amplifier configuration. It is also easy to provide a good input match so gain modules can be easily cascaded. The DA also gives a higher power level than amplifiers with a single stage, as the current generated by each active device is combined at the output collector line.

The major disadvantages of the amplifier are its relatively poor output power, noise figure and power added efficiency performance. In addition, the need for multiple active devices results in increased complexity and manufacturing costs. As the input signal propagates down the base line, each active device receives a reduced amount of input voltage compared to the previous one because the energy is dissipated by the device's base-emitter resistance. This effect is a function of frequency. Failure of any stage in the gain module will seriously affect the performance of the amplifier. This is because the gain is determined by the addition of signal from several HBTs.

2.5.6 Comparison of Broadband Amplifiers

A balanced amplifier is a good way to meet broadband requirements, but the use of quarter wavelength size couplers is not practical in MMIC's especially at low Gigahertz frequencies [67]. Distributed amplifiers are able to achieve a very broad bandwidth and ease in matching to the load, but suffer from low gain, low efficiency and relatively large chip size [63], [68]. Synthesizing the components with realistic values within a broad frequency band is extremely difficult in the low-loss matching designs [69]-[70]. Traditional amplifiers with lossy matching networks can be used to trade off the power gain for better gain flatness in a wider frequency range but undergo degradation in noise figure and output power [71]-[72]. A comparison of several broadband amplifiers is shown in Table 2.1.

Table 2.1: Comparison of broadband amplifiers

Amplifier Type	Advantage	Disadvantage	Typical bandwidth
Reactively matched	Best gain per stage, noise figure and output power	Difficult to control input and output VSWR Poor gain flatness when cascaded Sensitive to process variations	20% bandwidths at any centre frequency from 1 GHz to over 100 GHz Octave bandwidths just feasible
Lossy matched	Good VSWR and gain flatness Readily cascadable	Reduced gain per stage compared with reactive match Decrease in noise figure and output power	Octave bandwidths just feasible
Feedback	Excellent gain flatness over wide frequency range Good stability	Noise figure is mediocre and gain is reduced significantly High DC power consumption	0.1 to 6 GHz (MESFET) 6 to 18 GHz (MESFET) 20 to 50 GHz (pHEMT)
Distributed	Wide bandwidths achievable Good VSWR and easy to cascade	Low gain, mediocre noise figure and output power	1 to 20 GHz (MESFET) 1 to > 50 GHz (pHEMT) 1 >100 GHz (LM-HEMT)

In spite of having lower gain when compared with reactively or lossy matched amplifiers, distributed amplifiers can easily achieve more than one octave of bandwidth. In addition, there is poor gain flatness when using reactively matched amplifiers. Feedback amplifiers have a significant reduction in gain and high DC power consumption. Therefore, the most feasible broadband amplifier for this project is the distributed amplifier.

2.6 Operational Theory of DA

Using a simple amplifier model shown in Fig. 2.19, the forward gain of a travelling wave amplifier comprised of n active devices can be derived. The unilateral HBT is considered to be loss free and to consist of base capacitance C_{be} and a collector current generator I_n with associated collector capacitance, $C_{ce.}$ Other elements in the more general equivalent circuit are neglected to simplify the analysis. The artificial transmission lines form the input base line inductance, L_b and the output collector line inductance, L_c. The base and collector lines are terminated with their characteristic impedances, Z_b and Z_b respectively (assumed to be 50 ohms). The left-hand base port is terminated in a generator E_s having impedance $Z_{g.}$

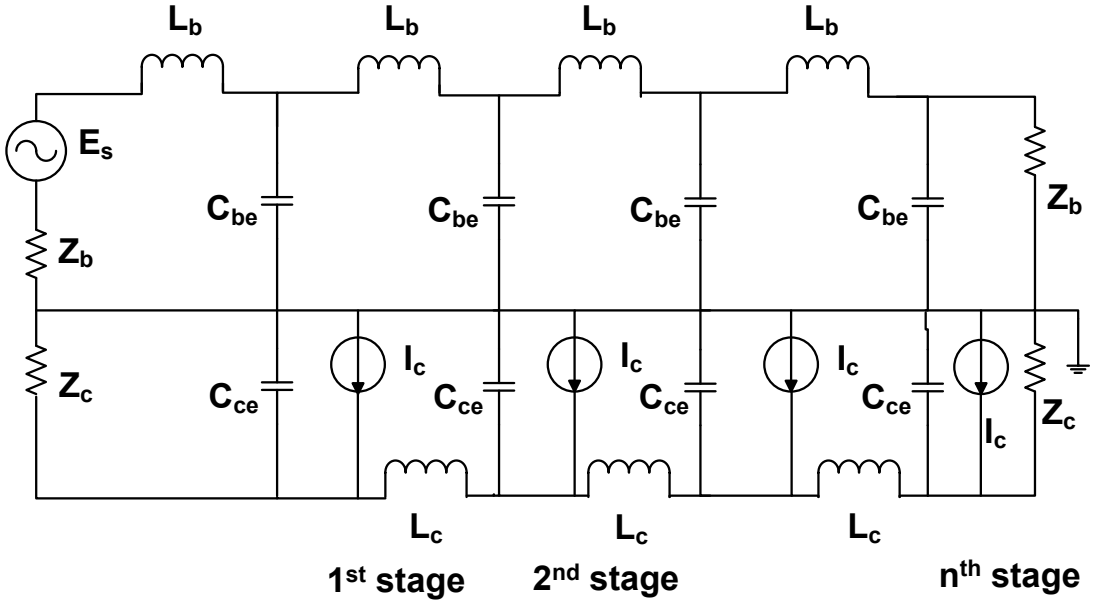

Figure 2.19: Travelling wave amplifier with n sections

A signal from the base generator propagates down the base line (with a phase constant β_b per section) and is dissipated in the right-hand base load, Z_b. The voltage across each base-emitter capacitor produces current $g_m V_{b,}$ in the collector line. The current from each HBT propagates down the collector line (with a phase constant of β_c per section). Power is dissipated in both the collector idle port load and the

amplifier output load. The forward gain (to the right-hand collector load) and reverse gain (to the left-hand collector load) can be calculated.

The total current I_C in the load Z_c is given by [73]

$$I_C = \frac{1}{2}\left\{I_n e^{-j\beta_c} + I_{n-1} e^{-2j\beta_c} + ... + I_1 e^{-jn\beta_c}\right\} \tag{2.21}$$

The voltage wave travelling down the base line due to E_s produces voltages $V_1, V_2 \ldots V_n$ across each base-emitter capacitor. If the voltage across the input terminals of the amplifier is V_{in}, then

$$V_1 = V_{in} e^{-j\beta_b}, V_2 = V_{in} e^{-2j\beta_b}, ..., V_n = V_{in} e^{-nj\beta_b}$$

Now

$$I_1 = g_m V_1, I_2 = g_m V_2, ..., I_n = g_m V_n$$

And

$$|V_1| = |V_2| = |V_n| = |V_{in}|$$

And

$$|I_1| = |I_2| = |I_n| = |I|$$

Therefore,

$$I_c = \frac{1}{2} V_{in} g_m \left\{e^{-j(n\beta_c+\beta_b)} + e^{-j(n-1)\beta_c+2\beta_b} + e^{-j(\beta_c+n\beta_b)}\right\} \tag{2.22}$$

This reduces to

$$I_C = \frac{1}{2} V_{in} g_m e^{-j(\beta_c+n\beta_b)} \left|\frac{1-e^{jn(\beta_c+\beta_b)}}{1-e^{j(\beta_c+\beta_b)}}\right| \tag{2.23}$$

But V_{in} is equal to ½ E_s since the amplifier is matched to the generator so that

$$|I_C| = \frac{1}{4} E_s g_m \left| \frac{\sin \frac{n}{2}(\beta_c - \beta_b)}{\sin \frac{1}{2}(\beta_c - \beta_b)} \right| \tag{2.24}$$

The power dissipated in the load Z_c is therefore given by

$$P_{load} = \frac{{E_s}^2 {g_m}^2}{16} \left| \frac{\sin \frac{n}{2}(\beta_c - \beta_b)}{\sin \frac{1}{2}(\beta_c - \beta_b)} \right|^2 Z_c \tag{2.25}$$

Since the power available from the generator is $E_s^2/4Z_b$ the available forward gain is given by

$$G = \frac{{g_m}^2 Z_c Z_b}{4} \left| \frac{\sin \frac{n}{2}(\beta_c - \beta_b)}{\sin \frac{1}{2}(\beta_c - \beta_b)} \right|^2 \tag{2.26}$$

If it is arranged that the propagation constants β_c and β_b are equal, then equation (2.26) simplifies to

$$G = \frac{n^2 {g_m}^2 Z_c Z_b}{4} \tag{2.27}$$

Thus for the case where $Z_b = Z_c = Z_o$

$$G = \frac{n^2 {g_m}^2 {Z_o}^2}{4} \tag{2.28}$$

2.7 Linearity and Nonlinearity

Nonlinearity is an inherent character of every electronic circuit. In weakly nonlinear circuits such as small-signal amplifiers, nonlinearities degrade system performance and must be minimized. On the other hand, frequency multipliers, exploit the nonlinearities in their design [74].

The superposition principle holds for linear circuits, where output to a signal composed by the sum of other more elementary signals can be given as the sum of the outputs to these elementary signals when taken individually [75]. This criterion can be applied to either circuits or systems. In mathematical terms, it can be stated as

$$y(t) = S_L\left[x(t)\right] = k_1 y_1(t) + k_2 y_2(t) \tag{2.29}$$

If

$$x(t) = k_1 x_1(t) + k_2 x_2(t) \text{ and } y_1(t) = S_L\left[x_1(t)\right], y_2(t) = S_L\left[x_2(t)\right] \tag{2.30}$$

This definition implies that only those frequencies present in the excitation waveforms are included in the response of a linear, time-invariant circuit or system. Linear, time invariant circuits do not generate new frequencies. (Time varying circuits generate mixing products between the excitation frequencies and the frequency components of the time waveform.) As nonlinear circuits usually generate a large number of new frequency components, this criterion separates linear and nonlinear circuits.

Nonlinearity in circuits are characterized as strongly nonlinear or weakly nonlinear. A weakly nonlinear circuit can be described by a Taylor series expansion of its charge/voltage (Q/V), nonlinear current/voltage (I/V) or flux/current (ϕ/I) characteristic around some bias current or voltage. This means that the characteristic is continuous, has continuous derivatives and does not require more than a few terms in its Taylor series. In addition, the nonlinearities and RF drive are weak enough that the DC operating point is not perturbed. Virtually all transistors and passive components satisfy this definition if the components are well below saturation. If a

circuit is weakly nonlinear, relatively straightforward techniques such as power series and Volterra series analysis can be used.

Strongly nonlinear circuits must be analyzed by harmonic balance or time domain methods. The general way of showing how new frequencies are generated in nonlinear circuits is to describe the component's I/V characteristic by a power series and to assume the excitation voltage has multiple frequency components [74]. Fig. 2.20 shows a circuit with excitation V_s and resulting current I.

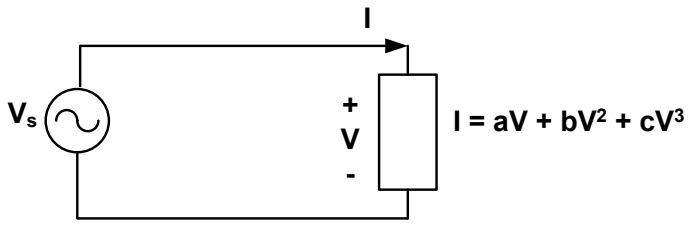

Figure 2.20: Two terminal nonlinear resistor excited by a voltage source

The current is given by the expression

$$I = aV_s + bV_s^2 + cV_s^3 \tag{2.31}$$

where a, b and c are constant real coefficients. V_s is assumed to be a two-tone excitation given by

$$V_s = v_s(t) = V_1 \cos(\omega_1 t) + V_2 \cos(\omega_2 t) \tag{2.32}$$

Substituting (2.24) into (2.23) gives, for the first term,

$$i_a(t) = av_s(t) = aV_1 \cos(\omega_1 t) + aV_2 \cos(\omega_2 t) \tag{2.33}$$

The second term after applying well-known trigonometric identities becomes

$$i_b(t) = bv_s^2(t) = \frac{b}{2}\begin{Bmatrix} V_1^2 + V_2^2 + V_1^2 \cos(2\omega_1 t) + V_2^2 \cos(2\omega_2 t) \\ + 2V_1V_2\left[\cos\left((\omega_1 + \omega_2)t\right) + \cos\left((\omega_1 - \omega_2)t\right)\right] \end{Bmatrix} \tag{2.34}$$

The third term gives

$$i_c(t) = cv_s^{\,3}(t) = \frac{c}{4}\begin{Bmatrix} V_1^{\,3}\cos(3\omega_1 t) + V_2^{\,3}\cos(3\omega_1 t) \\ +3V_1^{\,2}V_2\left[\cos\left((2\omega_1+\omega_2)t\right)+\cos\left((2\omega_1-\omega_2)t\right)\right] \\ +3V_1V_2^{\,2}\left[\cos\left((\omega_1+2\omega_2)t\right)+\cos\left((\omega_1-2\omega_2)t\right)\right] \\ +3\left(V_1^{\,3}+2V_1V_2^{\,2}\right)\cos(\omega_1 t) \\ +3\left(V_2^{\,3}+2V_1^{\,2}V_2\right)\cos(\omega_2 t) \end{Bmatrix} \quad (2.35)$$

The total current in the nonlinear element is the sum of the current components in (2.33) through (2.35). This current consists of a remarkable number of new frequency components, with each successive term generating more new frequencies than the previous one. By including a fourth or fifth order, the number of new frequencies generated would be even greater.

All the generated frequencies occur at a linear combination of the two excitation frequencies,

$$\omega_{m,n} = m\omega_1 + n\omega_2 \quad (2.36)$$

where m,n = ...,-3,-2,-1,0,1,2,3,... . The term $\omega_{m,n}$ is called a mixing frequency, and the current component at that frequency is called a mixing product. The sum of the absolute values of m and n is called order of the mixing product. For the m,n to be distinct, ω_1 and ω_2 must be noncommensurate. In other words, they are both not harmonics of a single fundamental frequency and it is a common assumption that the frequencies are noncommensurate when two or more arbitrary excitation frequencies exist. Table 2.2 shows the coefficients of the frequency terms that are generated when we substitute (2.32) into (2.31) and expand it to the fifth degree. It is clear from Table 2.2 that the odd-degree terms generate only odd-order mixing products and even-degree terms generate even-order products.

Table 2.2: Coefficients for frequencies generated due to nonlinearity

	a.V	**b.V^2**	**c.V^3**	**d.V^4**	**e.V^5**
1(dc)		1		9/4	
ω_1	1		9/4		25/4
ω_2	1		9/4		25/4
$2\omega_1$		1/2		2	
$2\omega_2$		1/2		2	
$\omega_1 \pm \omega_2$		1		3	
$2\omega_1 \pm \omega_2$			3/4		25/8
$2\omega_2 \pm \omega_1$			3/4		25/8
$3\omega_1$			1/4		25/16
$3\omega_2$			1/4		25/16
$2\omega_1 \pm 2\omega_2$				3/4	
$3\omega_1 \pm \omega_2$				1/2	
$3\omega_2 \pm \omega_1$				1/2	
$4\omega_1$				1/8	
$4\omega_2$				1/8	
$3\omega_1 \pm 2\omega_2$					5/8
$3\omega_2 \pm 2\omega_1$					5/8
$4\omega_1 \pm \omega_2$					5/16
$4\omega_2 \pm \omega_1$					5/16
$5\omega_1$					1/16
$5\omega_2$					1/16

2.8 Effects of Nonlinearity

The examination of new frequencies generated in nonlinear circuits give a description of nonlinear effects, especially to microwave systems. The previous power series techniques can show how they arise from the nonlinearities in individual components or circuit elements.

2.8.1 Harmonic Generation

A nonlinear system generates harmonics of the excitation frequency or frequencies. These are evident as the terms in (2.33) through (2.35) at $m\omega_1$ and $m\omega_2$. The mth harmonic of an excitation frequency is an mth-order mixing frequency. In narrowband systems, harmonics are not a serious problem because they are far from the signals of interest (in terms of frequency) and are rejected by filters.

2.8.2 Intermodulation Distortion

All the mixing frequencies in (2.33) to (2.35) that are linear combinations of two or more tones are called intermodulation (IM) products. IM products generated in an amplifier or communications receiver pose a serious problem, since they represent spurious signals that can be mistaken for the desired signals. Generally, IM products are much weaker than the signals that generate them. However, two or more very strong signals, which may be outside the receiver's passband, can generate an IM product that is within the receiver's passband and obscures a weak, desired signal. Even-order IM products usually occur at frequencies well above or below the signals that generate them, and consequently are often of little concern. The IM products of greatest concern are usually the third-order ones that occur at $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$, because they are the strongest of all odd-order products. These products are too close to the desired signals and cannot be rejected by filters.

2.8.3 Saturation and Desensitization

Equation (2.35) involves components at ω_1 and ω_2 that varied as the cube of signal level and are responsible for gain reduction and desensitization in the presence of strong signals. From (2.33) and (2.35), and with $V_2 = 0$, we find the current component at ω_1 designated $i_1(t)$ to be

$$i_1(t) = \left(aV_1 + \frac{3}{4} cV_1^3 \right) \cos(\omega_1 t) \tag{2.37}$$

From equation (2.37), the response current saturates if the coefficient c of the cubic term is negative (it does not increase at a rate proportional to the increase in excitation voltage). Saturation occurs in all circuits because the available output power is finite. If an amplifier is excited by a large and small signal, and the large signal drives the circuit into saturation causing gain to be decreased for the weak signal as well. Therefore, saturation also causes desensitization, which is a decrease in system sensitivity.

2.8.4 Cross modulation

The transfer of modulation from one signal to another in a nonlinear circuit is referred to as cross modulation. Assume that the excitation of the circuit in Fig 2.20 is

$$V_s = v_s(t) = V_1 \cos(\omega_1 t) + \big(1 + m(t)\big) \cos(\omega_2 t) \tag{2.38}$$

where $m(t)$ is a modulating waveform; $|m(t)| < 1$. A combination of an unmodulated carrier and an amplitude-modulated signal is defined in equation (2.38). Substituting (2.38) into (2.31) results in an expression similar to (2.35) for the third degree term, where the frequency component in $i_c(t)$ at ω_1 is

$$i_c'(t) = \frac{3}{2} cV_1 V_2^2 \big(1 + 2m(t) + m^2(t)\big) \cos(\omega_1 t) \tag{2.39}$$

where a distorted version of the modulation of the ω_2 signal has been transferred to the ω_1 carrier.

This transfer occurs because the two signals are simultaneously present in the same circuit, and depends strongly upon the strength of the interfering signal, ω_2 and the magnitude of the coefficient, *c*. An example of cross modulation can be seen by considering an automobile AM radio when one drives past the transmission antennas of a radio station. The modulation of that station momentarily appears to come in on top of every other received signal.

2.8.5 AM-to-PM conversion

AM-to-PM conversion is a phenomenon which causes a phase shift due to changes in the amplitude of a signal applied to a nonlinear circuit. This form of distortion can have serious consequences if it occurs in a system in which the signal's phase is important, such as in phase or frequency modulated communication systems. The response current at ω_1 in the nonlinear circuit element considered in Fig. 2.20 is from (2.33) to (2.35)

$$i_1(t) = \left(aV_1 + \frac{3}{4} cV_1^3 \right) \cos(\omega_1 t) \tag{2.40}$$

where $i_1(t)$ is the sum of the first and third order current component at ω_1. Assume, however, these components were not in phase. This possibility is not predicted by (2.31) through (2.35) because these equations describe a memoryless nonlinearity. In a circuit having reactive nonlinearities, it is possible for a phase difference to exist.

The response is then the vector sum of the two phasors given as

$$I_1(\omega_1) = aV_1 + \frac{3}{4} cV_1^3 \exp(j\theta) \tag{2.41}$$

where θ is the phase difference. The phase of I_1 changes with variations in V_1, even if θ remains constant with amplitude. It is clear from comparing (2.41) to (2.37) that AM-to-PM conversion is most serious as the circuit is driven into saturation.

2.8.6 Spurious Responses

A mixer, with an RF input at ω_{RF} and an LO at ω_{LO}, has currents at the frequencies given by

$$\omega = \omega_{RF} + n\omega_{LO} \tag{2.42}$$

can also be expressed by the notation

$$\omega_n = \omega_o + n\omega_{LO} \tag{2.43}$$

where n = …-2,-1,0,1,2,… and $\omega_o = |\omega_{RF}-\omega_{LO}|$ and is the mixing frequency closest to DC.

By applying RF at any of those mixing frequencies, currents at all the rest are generated as well. If the applied signal is very strong, its harmonics are generated and the mixer has spurious responses at any frequency that satisfies the relation

$$\omega_{IF} = m\omega_{RF} + n\omega_{LO} \tag{2.44}$$

where m and n can both be either positive or negative integers. Spurious responses can be seen as a form of two-tone intermodulation where one of the tones is the LO when we compare (2.42) to (2.44). In microwave technology, the concept of spurious responses is used only in reference to mixers.

2.8.7 Adjacent Channel Interference

In many communication systems, modulated signals are squeezed into narrow contiguous channels. Nonlinear distortion can generate energy that falls outside the

intended channel and this is called adjacent-channel-interference, spectral regrowth or sometimes co-channel interference.

Adjacent channel interference is fundamentally odd-order intermodulation distortion. Like most odd-order IM, it is dominated by third order effects, although higher order nonlinearities may also contribute to it. Volterra analysis of a weakly, nonlinear third order system shows that the output is the three-fold combination of excitation frequency components. These components fall close to the original excitation spectrum and cause adjacent-channel interference.

2.9 Common Linearization Methods

Linearity is always a key issue in designing a power amplifier. Modern communication systems can't afford to lose spectrum efficiency by disregarding amplitude modulation. However, with amplitude modulation, nonlinearity in amplitude introduced by an amplifier can result in spectrum regrowth and cause interference with adjacent channels. The amplitude modulation also introduces peak to average ratio (PAR) for the signal. For an amplifier to meet linearity requirement, input power has to be backed off according to the signal PAR. The larger the PAR, the more the amplifier needs to be backed off. Nevertheless, efficiency of the amplifier drops significantly by backing off the power. This is because power added efficiency of the amplifier can be obtained by referring to equation (2.1). By backing off the power, we are placing an upper limit to the output power, P_{outRF}. Therefore, power efficiency of the amplifier will drop as the output power is decreased. Thus, other linearization techniques are needed to improve linearity with less power back-off.

Generally speaking, all linearization methods can be categorized as either open-loop or closed-loop. Closed-loop systems are those involving feedback whereas those that do not such as predistortion is an example of an open-loop technique. The RF feedback and modulation feedback are classified under closed-loop techniques and modulation feedback and be further split into 3 sub-categories which are envelope feedback, polar loop and Cartesian loop. A third stand alone category is the

feedforward method which offers the precision of a closed-loop system but the stability and bandwidth of an open-loop system.

2.9.1 RF Feedback

In RF feedback, a portion of the RF output signal from the amplifier is fed back to and subtracted from the RF input signal without detection or downconversion [76]. The composite gain G of an amplifier with intrinsic gain of A having feedback network that subtracts a voltage βV_o from the input signal V_i, is given by

$$G = \frac{A}{1 + \beta A} \tag{2.45}$$

where A usually is assumed to incorporate a 180^o phase shift for a single stage low-frequency amplifier. The RF feedback amplifier is shown in Fig. 2.21.

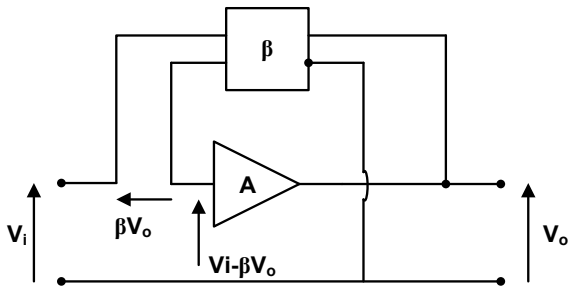

Figure 2.21: RF feedback amplifier

This feedback configuration desensitizes the overall amplifier gain G to any variations in the intrinsic gain A. The simplest way of expressing that is to differentiate (2.45) to find the rate of change of the composite gain G with intrinsic gain A.

$$\frac{\partial G}{\partial A} = \frac{1}{(1 + \beta A)^2} \tag{2.46}$$

so that

$$\frac{\delta G}{G} = \frac{1}{1+\beta A}\frac{\delta A}{A} \tag{2.47}$$

which shows that any fractional change in the intrinsic gain A will have an impact on the composite gain G, which will be reduced by a factor $(1+\beta A)$. This happens to be the same factor by which the negative feedback reduces the intrinsic gain A to the overall gain G.

Equation (2.47) means that by putting 10 dB of true negative feedback around any amplifier, the IM products, for the same output power will drop by 10 dB which is undesirable since much gain is lost. Another problem is that (2.45) assumes that the feedback process occurs instantaneously. There is no time delay between the occurrence of the output signal V_o and the voltage subtraction V_i-βV_o, The problem was stated in a classical paper on linearized VHF power amplifiers [77].

Negative feedback has been widely employed at low frequencies where stability of the feedback loop is easy to maintain [78]-[79]. The use of negative feedback at high frequencies has been limited by parasitic and time-delay effects, leading to instability problems. At wide bandwidths, stability and robustness problems will slow and constrain the use of feedback linearization [78], [80]. In an active RF feedback system, the voltage divider of a conventional passive feedback system is replaced by an active stage. While such systems demonstrate IMD reduction, they tend to work best at a specific signal level [81].

2.9.2 Modulation feedback

Modulation feedback techniques use some form of detection or demodulation to recover representations of the baseband modulating signal and power amplifier output signal. The difference between the two signals provides error signals which are used to apply correction to the amplifier control signals [82].

2.9.2.1 Envelope feedback

Envelope feedback corrects for AM-AM distortion and often applied to automatic gain control (AGC) loops to compensate for PA gain variations and to control pulse shaping in TDMA transmitters [83]-[84]. The RF input signal is sampled at the input and the output by a coupler and the envelope of the signals are obtained. The envelope are compared and subtracted from each other using a differential amplifier. The difference signal represents the AM distortion of the amplifier and this signal is amplified, filtered and used to modulate the driver stage of the PA.

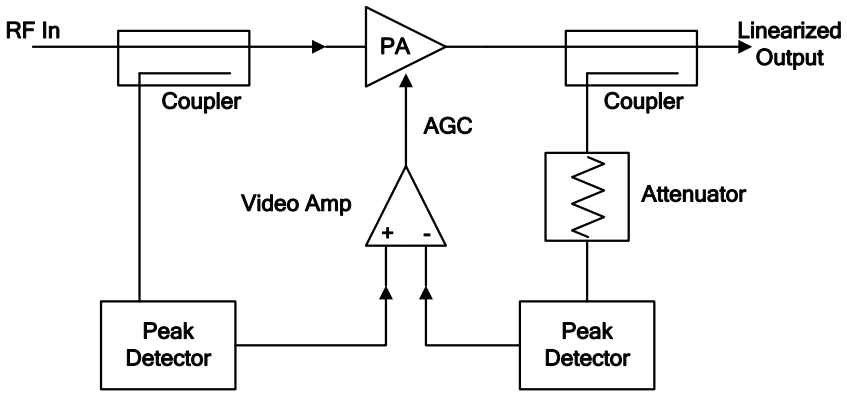

Figure 2.22: Modulation feedback system

Fig. 2.22 is an example of an envelope feedback system. This feedback method has been a mainstay of mobile communications industry for many years as a means of getting a few valuable dB of IM performance for VHF and UHF solid state power amplifiers [85]. Unfortunately, simple amplitude correction cannot increase the intrinsic power saturation of the device, so the effectiveness of the procedure will decrease significantly as the envelope swings into the compression region.

This technique does not correct for AM-PM effects. In fact, when implementing this technique, creating AM-PM distortion must be avoided. The delays in the detection and video signal processing can cause a video phase difference between the AM and PM processes, which reduce or even eliminate whatever correction may have been obtained by the amplitude feedback process. Techniques have been reported in

[86], which help optimize the feedback loop and avoid spurious oscillations and enables new ways for feedback linearization design.

2.9.2.2 Polar Loop

The polar loop is essentially an extension of the envelope feedback system described earlier but having both phase and amplitude correction. This technique is based around the principle of Envelope Elimination and Restoration (EER) but modified to allow feedback to be applied [87]. In [88], a polar loop implementation of the correction for an SSB transmitter has been reported. Although the system is a simple extension to the basic envelope feedback loop shown in Fig. 2.22, the block diagram is more complex. This is due mainly to the practical difficulties associated with measuring differential phase changes at a microwave signal frequency. The implementation shown in Fig. 2.23 uses a phased locked loop to maintain a constant amplifier phase transfer characteristic.

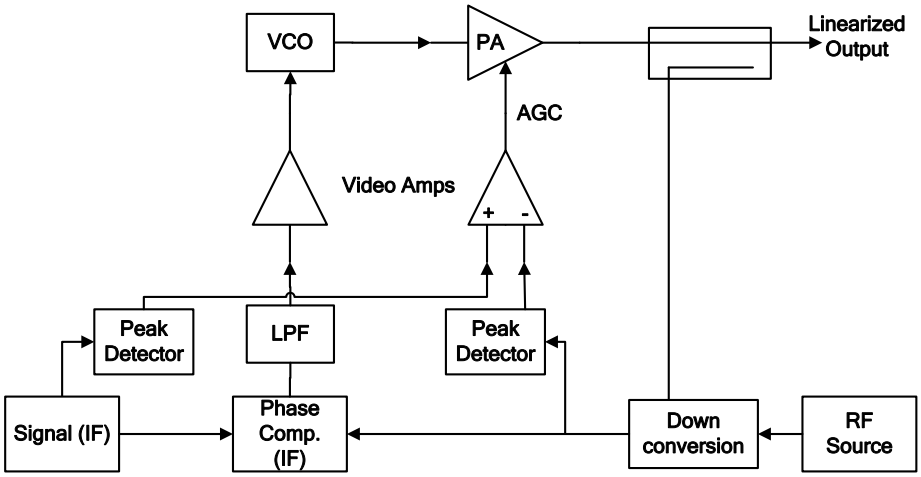

Figure 2.23: Polar loop system

One of the key issues with the polar loop is the different bandwidth requirements for the amplitude and phase error amplifiers. In practice, it is reported that the phase amplifier will require higher bandwidth. Therefore, differing levels of improvement for AM-AM and AM-PM characteristics usually occur and this causes poorer overall performance than the Cartesian loop technique. As with the envelope feedback loop,

the bandwidth limitations of the video circuitry will limit the usefulness of such systems to single-carrier applications.

2.9.2.3 Cartesian Loop

Cartesian correction has been reported to have some benefits over the polar loop technique [89]-[91]. It makes use of the fact that modulated RF signal can be represented in complex in-phase (I) and quadrature (Q) baseband form as well as by amplitude and phase functions. In a modern digital system, it is most likely that the baseband signal will already be available in I and Q format. Thus, the resulting I and Q channels can be processed in well-matched paths, eliminating the problems of the different bandwidth and signal processing requirements for magnitude and phase paths in the polar loop. Fig. 2.24 shows the essentials of a Cartesian loop linearization system.

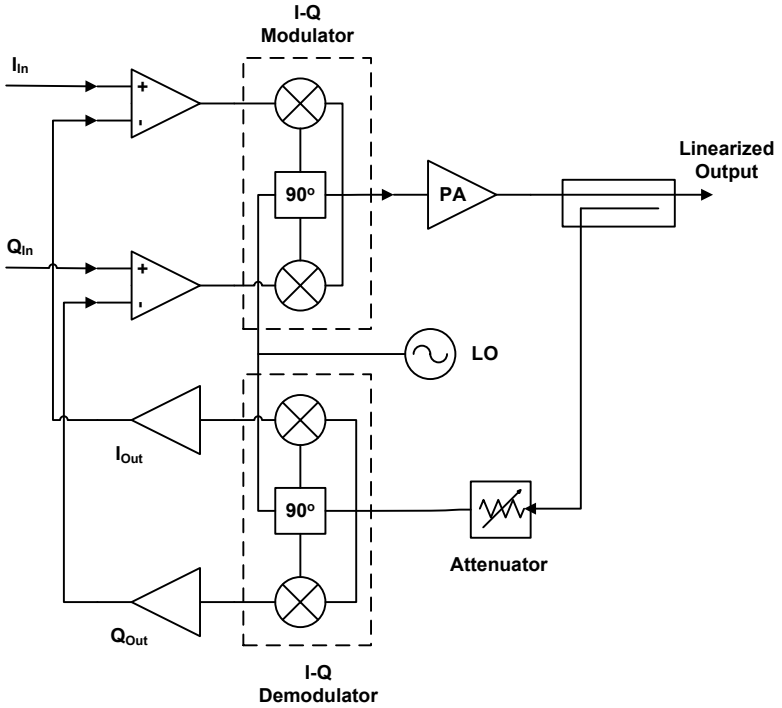

Figure 2.24: Cartesian loop system

The separate I and Q signal inputs will be the filtered, or smoothed, binary symbol sequences. The signals are fed through differential correcting amplifiers into vector modulators that form the actual RF signal *S(t)*, where ω_c being the RF carrier frequency, resulting in

$$S(t) = I(t)\cos\varpi_c t + Q(t)\sin\varpi_c t \tag{2.48}$$

The signal *S(t)* is then fed into the RF power amplifier, emerging with some distortion. A small portion of the output is coupled into a downconverter and retrieves the now distorted I and Q signals, which are then directly compared with the undistorted input baseband signals. The gain of the input differential amplifiers will force the loop into generating an output signal that closely tracks the original I and Q signals. The effectiveness of the Cartesian loop depends on the ratio of the feedback loop bandwidths to the I and Q input bandwidths and the linearity of the demodulators.

One of the benefits of the Cartesian loop over the polar loop is the symmetry of gain and bandwidth in the two quadrature signal processing paths. This will reduce the tendency to introduce phase shifts between the AM-AM bandwidth and stability will limit the capability to handle multicarrier signals. With the widespread availability of low-cost quadrature modulators and demodulators, the overall system becomes a simple linearized transmitter architecture. Cartesian loop transmitters that operate up to 900 MHz for relatively narrow band signals (<5 kHz bandwidth) with excellent results have been constructed [92]. The Cartesian loop also forms an entry point for digital linearization techniques.

2.9.3 Predistortion

Predistortion is the most commonly used method that falls under the separate heading of open-loop linearization techniques. Open-loop techniques have the disadvantage of reduced precision over closed-loop systems, but they have the advantage of much greater linearization bandwidth since it does not have to deal with the parasitics and time-delay introduced by the feedback loop. Stability issues are effectively absent and

it also tends to be cheap, typically consisting of simple module containing a few carefully optimized components. Predistortion techniques are superior in terms of its wideband performance [93] and RF predistorters based on diode or transistor devices have been implemented for wideband systems [78]-[80].

Predistortion techniques attempt to modify the incoming signal to complement and cancel the nonlinear effects in PAs. Historically, these techniques has been aimed primarily at AM-PM correction, particularly in TWTs, which to this day perform broadband amplification feats untouched by the solid state revolution in military ECM applications. There is an extensive literature on the subjects [94]-[95], but only limited to applications in narrowband systems. Predistortion can be classified as gain and phase, nonlinear generators or baseband predistortion.

1) Gain and phase predistortion

   The simplest predistorters use expansive networks to compensate for the gain compression experienced by a power amplifier as the operating point approaches the 1 dB compression point. These networks are typically diode-resistor networks and can achieve 5 to 15 dB reduction in third order IM distortion [96]. An RF level-dependent resistor, combined with a fixed capacitor, can give a suitable AM-to-AM and AM-to-PM characteristic that opposes the distortion of the amplifier in the pre-compression zone. This can result in as much as a 5 dB improvement in ACP [97].

   An alternative approach is to place voltage-controlled attenuators and phase shifters in the input path and use the envelope of the RF signal to dynamically adjust the settings. Typical improvements in third order product are up to 10 dB, but as with all open-loop correction systems, it is sensitive to temperature, amplifier gain and some form of adaptation is often required.

2) Predistortion using nonlinear generators

   Using nonlinear generators, complementary IMD can be generated and used to cancel the PA distortion [17]. Several ways are used to implement this method with the simplest being a diode or transistor network in series with the main

signal path. Another alternative is to apply feedforward predistortion using a low power transistor with similar distortion characteristics as the main amplifier. With care, it is possible to achieve 15 dB reduction in third order products.

3) Baseband predistortion

By using digital signal processing (DSP), predistortion to the baseband modulation signals can be applied prior to upconversion and greater precision can be obtained [98]. The mapping based predistorter uses a large look-up table to map the input I and Q signals to new predistorted values [99]. Another form of baseband predistortion is by using the gain-based predistorter. It uses the envelope level to modify the complex output signal with interpolation between stored values. The third alternative is analog-based predistortion where the correction is applied to the baseband signals with analog circuits.

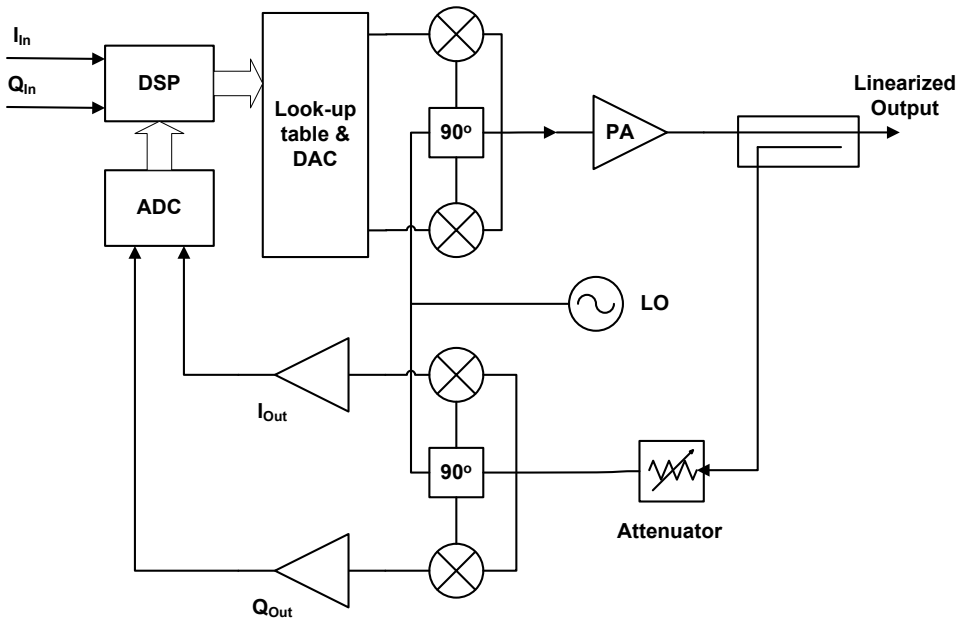

Figure 2.25: Digital adaptive predistortion system

Fig. 2.25 shows a block diagram of an adaptive digital predistortion loop. In a normal operation, the system works as an open-loop predistortioner, with the lookup table providing a preprogrammed I-Q output pair for each input envelope sample. The

I-Q output pair contains the appropriate phase and amplitude correction required to compensate for the PA nonlinearity at the current signal level. Because of the precision of the DSP, such systems have been reported to give impressive corrections, as measured in reduced IM or ACP levels [100], but even in open-loop mode they operate too slowly for some applications. The DSP circuitry also can consume too much power for lower power PA applications.

Digital predistortion is a dominant choice in contemporary base station amplifier designs. It provides very good performance and great flexibility by using an adaptive digital closed-loop control [101]. Advanced algorithms such as the genetic algorithm can be used to improve computation efficiency in the digital domain. However, using digital predistortion for handset amplifiers is still not popular due to the concerns of circuit complexity and cost.

Analog predistortion is still the only viable ways to achieve linearity improvement in a compact handset power amplifier, although it only achieves moderate linearity improvement and usually cannot adapt over a wide dynamic power range or wide temperature change. A diode based analog predistortioner was presented in [102]. If the nonlinear gain and phase transfer functions introduced by the diode are inverse to those of the power amplifier following it, the input signal can be properly predistorted. This method is really popular in practice because of its simplicity and its ability to enhance maximum output power by 1-2 dB, where efficiency and linearity of the amplifier matter the most. By having the same output power, a 1-2 dB enhancement from the predistortioner translates to 25-50% saving of active device area.

2.9.4 Feedforward

Feedforward is an old technique, dating back to the original feedback patent proposed in [103]. It is merely a different implementation of the same basic concept as feedback except that the correction is applied to the output, rather than the input of the amplifier. In that manner, the time causality conflict of direct feedback is removed along with of instability and bandwidth limitations [77], [104].

Feedforward stands alone as the only viable linearization technique that combines the precision of a closed-loop correction system with the bandwidth required for multicarrier applications. However, there are trade offs involved. In applying the feedback correction at the output of the amplifier, outside the correction loop, the correction signals need to be amplified up to the necessary higher power level. Great accuracy in gain and phase tracking also needs to be maintained in the different elements of the system. Other issues on feedforward amplifiers include effects of imbalances and imperfect cancellation, stability, controller loop and optimizing algorithm. [105]-[107].

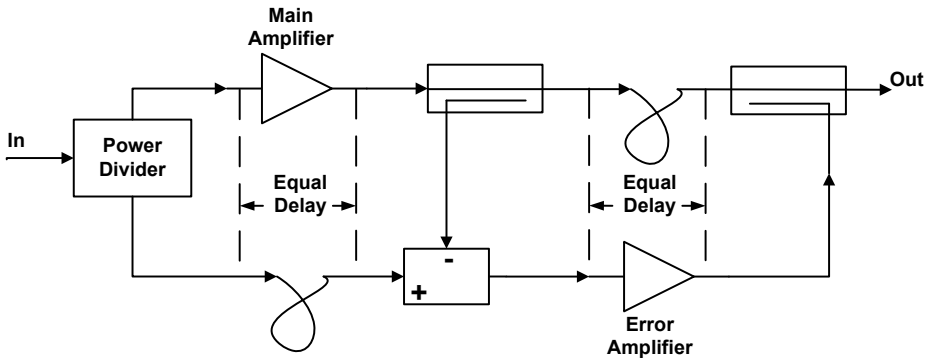

Figure 2.26: Basic feedforward correction loop

Fig. 2.26 shows a basic feedforward correction loop. A delayed sample of the undistorted input signal is compared with a coupled and suitably attenuated, sample of the output signal using a 180^{o} combiner. If the amplifier has no gain or phase distortion, the combiner will produce zero output. Any gain or phase distortion in the amplifier, in the form of compression or AM-PM effects, will result in a small RF error signal at the output of the combiner. The error signal is amplified back to the original level at which the output sample was taken and is recombined with the output, following a delay line in the main signal path that compensates for the delay in the error signal amplifier.

The key aspects to note in the basic correction process are that both amplitude and phase errors are removed and that the addition and subtraction process is performed at RF, rather than at video or baseband. That means the correction process operates over a bandwidth ultimately defined by the phase and amplitude tracking of the various

components of the system. Even by using advanced amplifiers structures like Doherty amplifiers to improve efficiency at the main amplifier in the feedforward system, overall efficiency is still limited by the drawbacks inherent in the feedforward structure [108]. Feedforward techniques reported in [82], [109] rely on automatic compensation loops based on analog solutions and digital adaptive compensation.

2.9.5 Low impedance termination method

Unlike the Cartesian loop and predistortion which are system level linearization methods, the low impedance terminations can be applied to one particular device such as a power amplifier. This means it has the potential to be used in conjunction with the other system level linearization techniques to bring more improvement in linearity. Low impedance networks are applied to tune out the second harmonic ($2\omega_2$) and envelope frequencies (ω_2-ω_1) since third order intermodulation products are dependent on the components at these frequencies [10]-[11], [110].

According to K.L. Fong, using a low frequency trap network increases the linearity of a BiCMOS LNA by 8.35 dB at 2 GHz and 7.25 dB at 900 MHz [9]. By using the Volterra series, he is able to explain the linearity improvement phenomenon caused by the trap networks at the input of inductively degenerated common-emitter transconductance stage. V. Aparin and C. Persico successfully increased the IIP3 by 14 dB by tuning the input matching network of a 2 GHz Si BJT LNA at the sub and second harmonic frequencies without affecting the in-band gain, noise figure and return loss [10]. The out-of-band terminations can be optimized for lower third order intermodulation using a derived closed form expression and it is possible to achieve higher IIP_3 in the same frequency range by optimizing the input matching network for multiple second harmonic frequencies.

A SiGe BiCMOS operating at 0.88 GHz has been linearized to achieve IIP3 of 11.7 dBm by resorting to a low-frequency low-impedance termination [11]. The work also shows that the technique is effective in linearizing BJTs but not for FETs if it is biased in the strong inversion region. Shorting the RF input at low frequencies of up to ω_2-ω_1 of a Si CMOS LNA at 1.96 GHz results in a 9 dB increase in the IIP3 [12].

This is implemented by a DC bias boost circuitry that provides the low impedance at the envelope frequency.

Applying optimum source impedance can provide linearity improvements of up to 8 dB for a common emitter BJT stage at 1.8 GHz [13]. When used together with predistortioners, its cancellation performance will significantly improve since the memory effects caused by the stage and predistortioner can be partially cancelled by providing optimum source impedances at different envelope frequencies. A novel load-pull method for envelope termination has been applied to linearize a LDMOS transistor at 850 MHz [111]. This work also shows that the optimum envelope termination is complex contrary to the popular belief that the envelope termination must be approximately zero. It should be noted that the Third Order Input Intercept Point (IIP3) is equal to Third Order Output Intercept Point (OIP3) without the amplifier gain. So the amount of improvement in terms of IIP3 is the same for the OIP3.

There are generally three ways to implement low impedance terminations. They are by using LC trap [9], active inductor [12] or a bias choke [11]. The traps can be a dedicated network shown in Fig. 2.27 (a) or part of the input matching components shown in Fig 2.27(b). In the former, the L creates a high impedance at the fundamental frequencies to avoid interfering with the in-band performance of the amplifier whereas in the latter, the L can be a matching inductor. The C functions to resonate with the L at the envelope frequency. A large capacitor value (several μF is required) to cover lower envelope frequencies (usually kHz range). Selecting a large value capacitor slows down the gain switching time due to the charging and discharging of the capacitor. However, if gain switching is not important, this method is attractive due to its simplicity and negligible effect on noise figure, gain and stability.

Gain switching time can be reduced by using an active inductor bias shown in Fig. 2.28 (a). The circuit uses an operational amplifier with negative resistive feedback which isolates the opamp input and output from the signal path at the fundamental frequency. The major challenge of this design is ensuring the opamp has enough gain

at the highest frequency affecting the LNA cross modulation distortion which is the separation frequency of the transmit and receive channels. This is difficult to satisfy without trading off the opamp phase margin. Thus, the bias circuit often shunt the LNA input causing lower gain and higher noise figure.

By using an RF choke to isolate the opamp from the LNA input, a compromise between the opamp stability and LNA performance can be achieved. This is shown in Fig. 2.28 (b). Since there is no need for a large capacitor, the gain switching can be very fast.

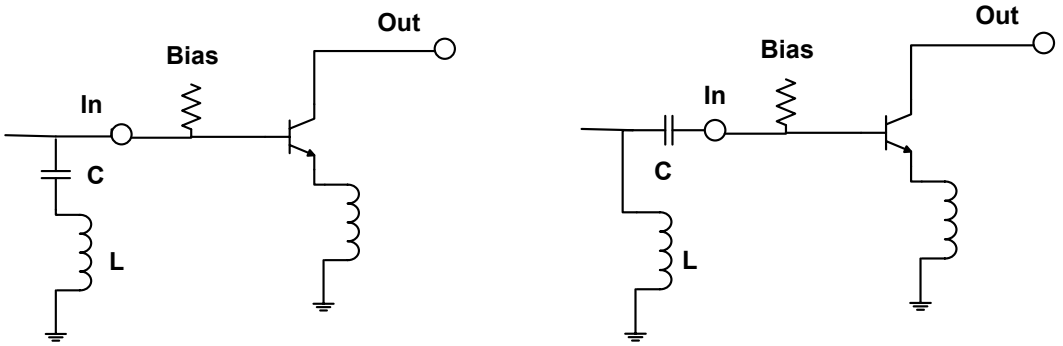

Figure 2.27: (a) LC trap network 1 (left)

(b) LC trap network 2 (right)

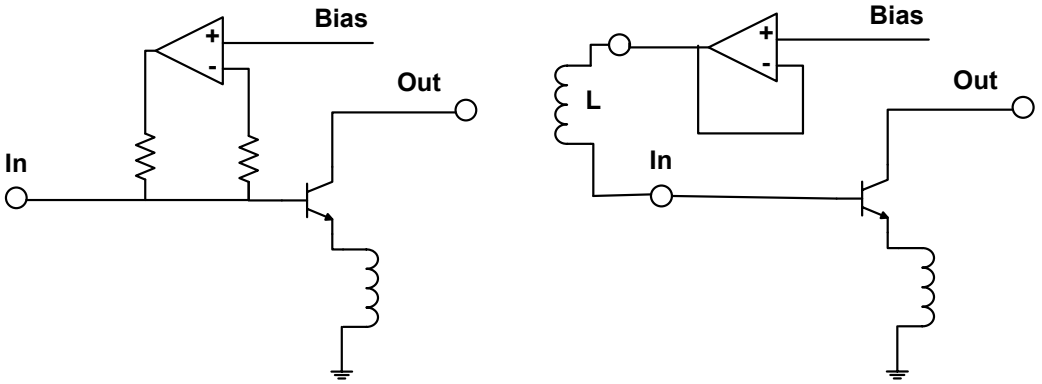

Figure 2.28: (a) Active bias network (left)

(b) Bias choke network 2 (right)

From the three techniques of low impedance terminations, the LC trap method is chosen since gain switching time is not the issue that is meant to be solved in this project. The simplicity of the LC trap makes it easier to implement and tune since the external L and C SMT components soldered on the testboard needs to be removed and changed. This is to examine the optimum termination needed to provide the highest linearity.

The area of improvement that can be applied to the LC trap method is to implement it over a broadband of frequencies. To date, this method has been reported to provide linearity improvement only in a narrowband. However, these traps must be modified to provide low impedance at only the envelope frequencies and not the second harmonic in order for it to work over a broad bandwidth. The traps shall be tested at the input and output of the HBT to view its effects. Previous linearization research has been carried out by placing optimum terminations at the input [9]-[13] and output [111]. The optimum trap values to maximize linearity shall also be tested by varying the inductance and capacitance of the trap since [111] has already proven that it is not zero. According to [112], an optimum bias condition exists for minimize third order distortions due to the bias dependence of the nonlinear base-collector charge. Therefore, measurements shall be taken with three different base bias voltages. Since the traps are designed to short out the envelope frequencies, the effects of varying the spacing between the two input signals while maintaining the center frequency is also scrutinized.

2.9.6 Comparison of Linearization Methods

Closed-loop systems, which would include various forms of feedback, can provide high levels of linearization, but seriously limited in terms of modulation bandwidth. This can be a restriction even in single channel transmitter applications, in which modern digital modulation schemes can run into the megahertz range at the baseband. This also rules out its use for multichannel applications, in which the effective modulation bandwidth becomes a function of the RF carrier separation. Direct RF signal feedback is hard to achieve in reality because it requires a fast feedback loop to

maintain loop stability. Cartesian feedback is an old concept and was popular in base-station amplifier design for some time. However, there are only a handful of successful examples in which it is implemented for a compact integrated amplifier such as the work by J.L. Dawson involving a novel phase alignment loop [113].

Open-loop systems such as predistortion typically never have the correction precision of a closed-loop system but they potentially have the capability of handling much wider modulation bandwidths including multicarrier signals. They also have no inherent stability problems, which are another fundamental limitation in closed-loop systems.

The feedforward system stands alone in a third category and can in principle offer the precision of a closed-loop system and the stability and bandwidth of an open-loop system. However, there is a trade off, which presents itself in the form of challenging gain and phase tracking requirements and poor overall efficiency due to the need for an additional power amplifier in the correction loop. This makes feedforward undesirable especially in high volume production environment.

The methods mentioned above are mainly system level techniques that have their own pros and cons. This project seeks to use the LC trap method to linearize a single component (Distributed Amplifier) and can be used in conjunction with the other system level techniques described above. So far, work has only been published regarding the use of LC traps to linearize a narrow bandwidth [9]-[13], [111]. The novelty of this project is to improve the linearity over a broadband by implementing the LC trap method.

The LC envelope trap method generally can provide linearity improvement over a larger bandwidth compared to the closed-loop (feedback) method and is much simpler and cost-effective to implement compared to predistortion and feedforward techniques. It also does not affect the efficiency of the device. The only drawback using the LC trap is that it might cause instability since they short out the low frequencies. These traps must be carefully designed so that the amplifier is still stable after its implementation. A comparison of the linearization techniques is shown in Table 2.3.

Table 2.3: Comparison of existing linearization techniques

Linearization Technique	RF bandwidth	Linearity Improvement	Efficiency	Complexity	Drawback
Power backoff	Wide	High	Low	Low	Very low efficiency
RF Feedback	Narrow to Moderate	Low	Low	Moderate	Low gain
Envelope Feedback	Moderate	Low	Moderate	Low	Stability problems
Polar Loop	Narrow to Moderate	High	High	High	Stability problems
Cartesian Loop	Narrow to Moderate	High	High	Moderate to High	Stability problems
Gain and phase Predistortion	Moderate to Wide	Low	High	Moderate	Low correction precision
Nonlinear Generator	Moderate to Wide	Low	High	Moderate to High	Low correction precision
Baseband Predistortion	Moderate to Wide	Low	High	Moderate to High	Low correction precision
Feedforward	Wide	High	Low	High	Difficult gain and phase tracking
LC Envelope Trap	**Wide**	**Moderate**	**N/A**	**Low**	**Stability issues**

2.9.7 Summary

In this chapter, the characteristics of the power amplifier have been explained which includes the OIP3, a figure of merit for linearity. Linearity is a property of the PA that must be increased since it determines the signal integrity of the system. A brief explanation of HBTs and how they operate are also included. HBTs are similar to BJTs except that they incorporate a heterojunction at the base-emitter junction. The heterojunction consists of materials with the similar lattice constants but with different energy gaps such as InGaP with GaAs. Compared to silicon, GaAs can achieve higher breakdown voltage and higher output power. It is normally used for

high speed communication systems due to its high electron velocity and mobility. Furthermore, GaAs also has a lower substrate loss compared to silicon.

Comparisons of several architectures of broadband amplifiers are also included with focus on the distributed amplifier. The DA has lower gain when compared with reactively or lossy matched amplifiers but can easily achieve more than one octave of bandwidth. In addition, there is poor gain flatness when using reactively matched amplifiers. In addition, feedback amplifiers have large reduction in gain and high DC power consumption, making the DA the most feasible architecture for this project.

Due to the nonlinear nature of power amplifiers, it will produce several effects such as harmonic generation, intermodulation distortion, saturation, desensitization, cross modulation, AM-to-PM conversion and adjacent channel interference. Third order intermodulation products are the most detrimental to a receiver since the form very close to the desired signals and cannot be removed by a filter. To reduce these third order products, the linearity of the PA must be increased.

Linearity and output power can always be traded off with one another. However, it is desirable to provide higher levels of linearity while maintaining a high level of output power. This motivation has led to many techniques being implemented such as RF feedback, envelope feedback, polar loop, Cartesian loop, predistortion and feedforward. These techniques can be classified as system level techniques since they are implemented at the system rather than a particular device. Techniques which involve feedback can provide high levels of linearization but lack in terms of the bandwidth in which the technique can be applied. On the other hand, predistortion never have the correction precision of a feedback system but they have the capability of handling much wider bandwidths.

Although feedforward solves the two drawbacks of the feedback and predistortion methods, it is much more difficult to implement and cause the system to suffer from poor efficiency. The LC trap method is more of a device level technique and can be used together with the other system level techniques described above. To date, research papers have only been published regarding the use of LC traps to linearize a narrow bandwidth. By using the LC trap method but modified to work only with the

envelope frequency, linearity improvement can be achieved over a larger bandwidth compared to the feedback method and is much simpler to implement compared to predistortion and feedforward techniques. It also does not affect the efficiency of the device.

CHAPTER 3
METHODOLOGY

3.1 Introduction

This chapter starts by explaining in detail the design methodology applied to the first and second design iterations of the DA. Two separate design iterations must be carried out to examine the effects of placing traps on the input and output of the DA. The second DA design has bond pads which go directly to the input of the HBT, bypassing the equalization capacitor. Preparatory steps for the MMIC before the measurement process such as die attach, wire-bonding and testboard population concludes this chapter. To demonstrate how the input and output traps work in reducing the third order products, an analysis is shown with nonlinear HBT models. The simulation, measurement and verification setups are included as well.

3.2 First Design Iteration of Distributed Amplifier

For the first design iteration, the MMIC are fabricated using the WIN Semiconductor Corporation's H02U-41 InGaP/GaAs HBT foundry process [114]. Using the design kit supplied by the foundry, schematics and layouts for the MMIC DA were designed using Agilent's Advanced Design System (ADS) CAD program. The first and second design iterations have a bandwidth of 0.5 to 3.0 GHz and must achieve a minimum gain of 10 dB and a minimum P_{1dB} of 17 dBm (~50 mW). Achieving an increase in linearity will not be considered a success if the DA cannot provide the specified gain and output power. These requirements have been chosen since the DA is expected to cover the frequencies for cognitive radio, GSM up to license-free WiMAX (at 2.4

GHz). By following the gain-bandwidth product, the gain should be roughly around 10 dB, given that the upper frequency is 3.0 GHz and the transit frequency or unity gain frequency, f_t is 31 GHz (Gain X Frequency = f_t). A P_{1dB} of roughly 17 dBm is reasonable for a broadband DA. The LC traps implementation for narrowband improvement in linearity shorts out both the second harmonic ($2\omega_2$) and envelope frequencies. However, in order to maintain the in-band performance of the DA, the traps in this project must provide low impedance only at the envelope frequency.

3.2.1 Selection of Active Device

The most important component of a successful distributed amplifier design is a high performance transistor. The MMIC designer has freedom over the number of sections and the layout of the interconnecting lines of the transistor, but the basic transistor performance determines the maximum gain/bandwidth performance that can be achieved.

Since the base-emitter capacitance is considerably larger than the collector-emitter capacitance, this will determine the cut-off frequency and thus the maximum frequency of operation. A higher cut-off frequency could be achieved by using an HBT with a lower C_{be}, but the transconductance g_m, would also be correspondingly lower, giving less gain. Likewise, a larger device has higher g_m and gives more gain, but the higher C_{be} lowers the cut-off frequency.

This can be proven by considering two equivalent circuit models for the HBT placed in parallel shown in Fig. 3.1. Having a larger device is the same as placing smaller devices in parallel with each other. Since the base-emitter capacitance, C_{be} are in parallel, they add up and is higher for larger devices. Transconductance, g_m is given by

$$g_m = \frac{\Delta I_{out}}{\Delta V_{in}} \tag{3.1}$$

The ΔV_{in} stays the same with that of a single device but the ΔI_{out} doubles due to the contributions of the collector current from the two devices. Therefore, g_m is dependent on device area and is higher for larger devices too.

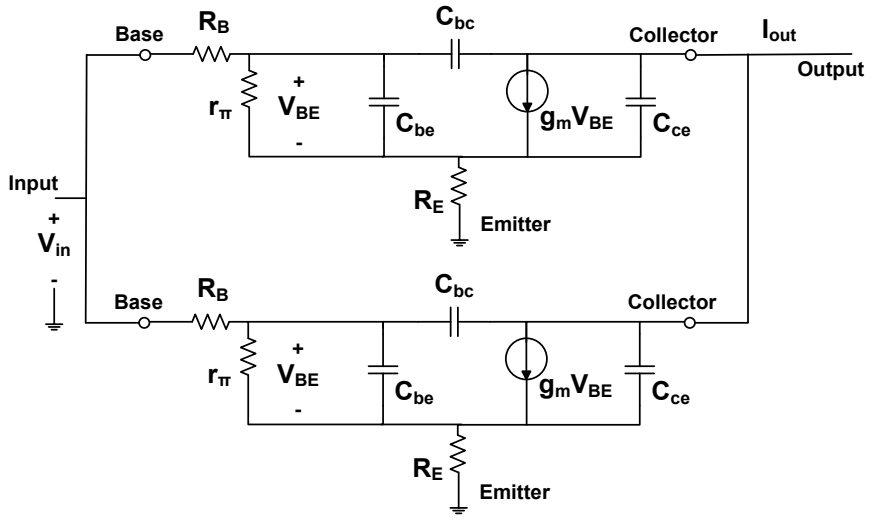

Figure 3.1: Two equivalent circuit models for HBT connected in parallel

One consideration in this geometry is the amount of heat that is generated. The number of emitter fingers and total current must not be too great. The choices for the HBTs (by emitter periphery) are:

i. 2 μm X 2 μm X 1 finger
ii. 2 μm X 20 μm X 1 finger
iii. 2 μm X 20 μm X 2 fingers
iv. 3 μm X 40 μm X 1 finger
v. 3 μm X 40 μm X 3 fingers

To achieve the best trade off between gain and bandwidth, the transistor selected is the WIN Semiconductor's RQ1A202F2_M2 HBT transistor. It has a two emitter fingers with the width and length of each emitter mesa are 2 μm and 20 μm respectively, giving an emitter periphery of 80 μm^2. Furthermore, the emitter fingers connect within the device by the first metal as shown in its layout in Fig. 3.2. Table 3.1 indicates the basic parameters for the transistor.

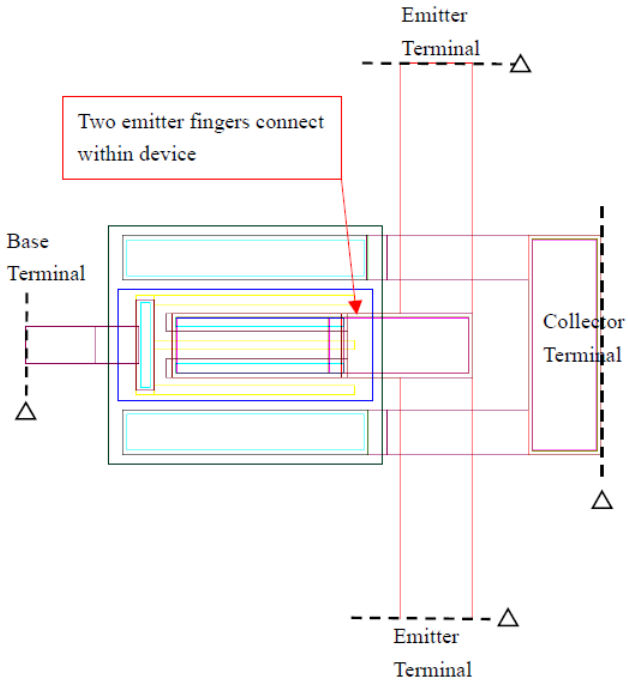

Figure 3.2: Layout RQ1A202F2_M2 HBT transistor [114]

Table 3.1: Parameters for RQ1A202F2_M2 HBT transistor

Parameter	Value
BV_{CBO}	30 V
BV_{CEO}	17 V
BV_{BEO}	7 V
Maximum I_C	32 mA
Nominal bias	12 mA
Peak f_T	31 GHz
Peak f_{max}	110 GHz

3.2.2 Selection of Bias Point

There are several classes of operation for an amplifier. The class A amplifier gives the highest linearity since no waveform clipping is introduced before the amplifier saturates. However, the trade off is its efficiency with only a peak efficiency of 50% if inductive biasing is used and 25% if resistive biasing is used [115]. This is due to the

fact that it is always on and has a constant conduction angle of 360°. DC current is always flowing regardless of whether RF current is flowing or not.

Fig. 3.3 shows the collector current, I_C versus the collector-emitter voltage V_{CE} simulated in ADS using the model of the RQ1A202F2_M2 HBT transistor from [114]. For a class A operation, the amplifier must be biased in the middle of the current-voltage characteristics (shown in Fig. 3.3). Therefore, V_{ce} is fixed to 5 V and the V_{BE} is set to 1.375 V. For DA1 and DA1B, V_{be} of 1.375 V results in a base current of 128 μA and 111 μA respectively. This is simulated and shown in Fig. 3.4. Note that DA1B is from the second design iteration DA which is shown in Section 3.5.

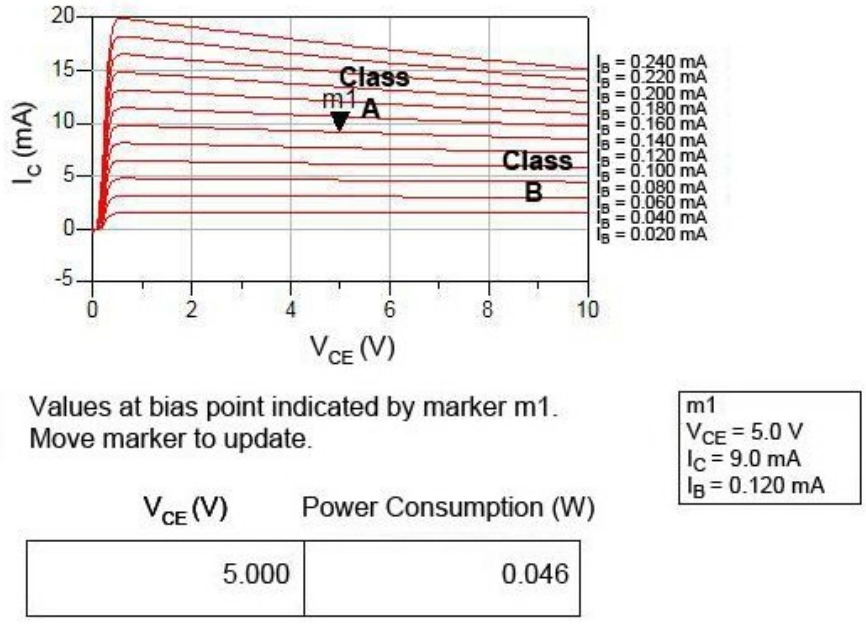

Figure 3.3: Current-voltage characteristic for RQ1A202F2_M2 HBT

DA1

freq	X1.Base_current.i	Collector_current.i
0.0000 Hz	128.4 uA	78.36 mA

DA1B

freq	X1.Base_current.i	Collector_current.i
0.0000 Hz	111.1 uA	55.66 mA

Figure 3.4: Base and collector currents for DA1 and DA1B simulated in ADS

3.2.3 Unit Cells

The DA is made up of several sections and each section has an identical unit cell. Four design variants DA1 to DA4 were considered for this project. DA1 and DA2 utilize parallel ballasting whereas DA3 and DA4 apply series ballasting. Figs. 3.5 and 3.6 below show the schematic for the unit cells in ADS. Ballast resistors are indicated by $R_{bal.}$ These unit cells are cascaded in the overall design of the MMIC DA and will be shown in Section 3.2.4. Paths to ground are implemented using backvias through the GaAs circuit substrate.

From Figs. 3.5 and 3.6, the input signal is split into two base lines. The HBTs from the two base lines are excited and combined into a single collector line. This results in doubling the total base periphery without affecting the loading on the base line. Furthermore, the load line impedance is halved since there is twice the collector periphery on the output line.

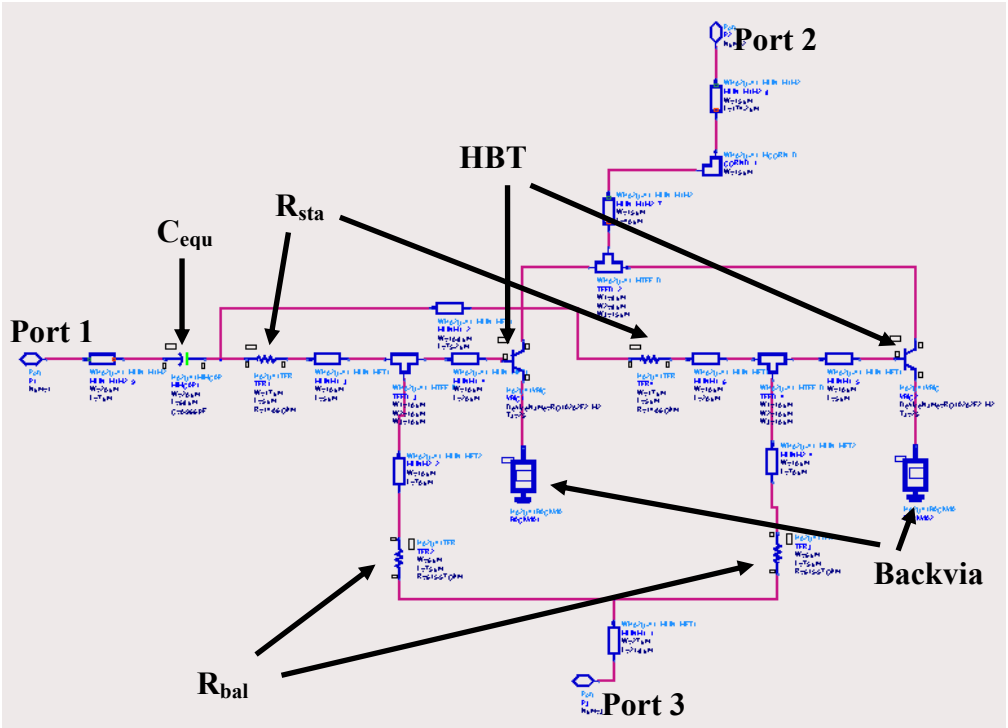

Figure 3.5: Unit cell schematic for DA1 and DA2 (parallel ballast)

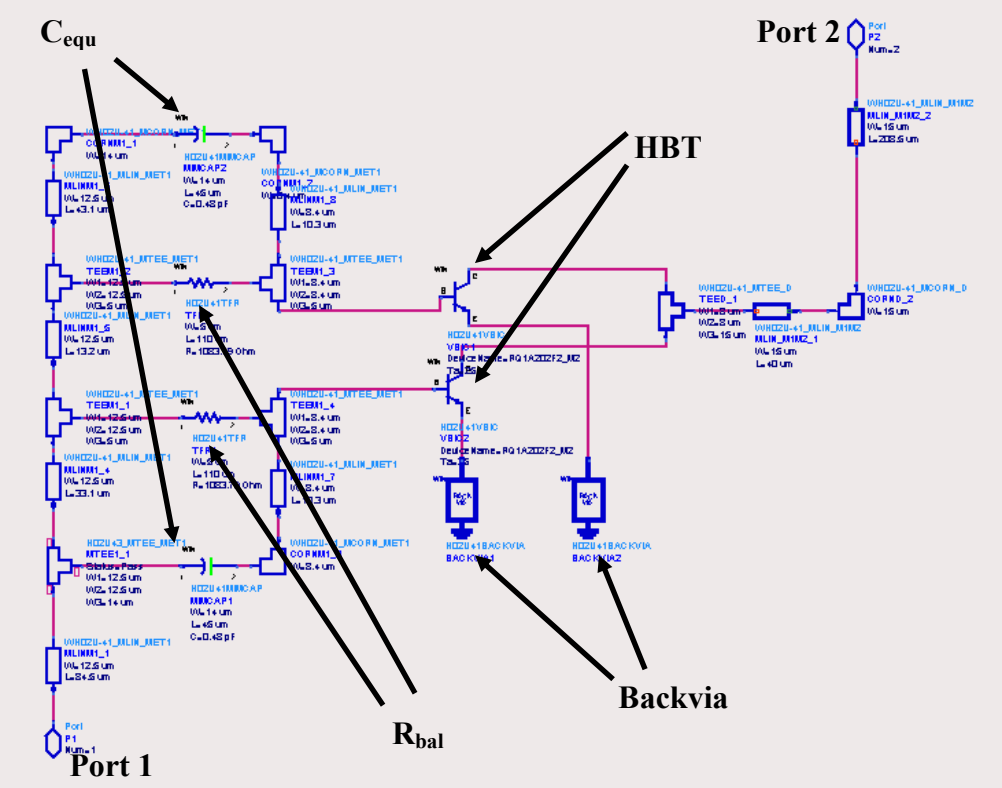

Figure 3.6: Unit cell schematic for DA3 and DA4 (series ballast)

Table 3.2 shows the component values indicated in Figs. 3.5 and 3.6.

Table 3.2: Component values for unit cells (First design iteration DA)

DA	Component	Size (Width X Length)	Value
DA1 (Parallel ballasting)	C_{equ}	20 µm X 68 µm	0.966 pF
	R_{sta}	17 µm X 5 µm	14.06 Ω
	R_{bal}	6 µm X 75 µm	615.57 Ω
DA2 (Parallel ballasting)	C_{equ}	30 µm X 68 µm	1.392 pF
	R_{sta}	22 µm X 5 µm	10.79 Ω
	R_{bal}	6 µm X 75 µm	615.57 Ω
DA3 (Series ballasting)	C_{equ}	14 µm X 45 µm	0.48 pF
	R_{bal}	5 µm X 110 µm	1083.79 Ω
DA4 (Series ballasting)	C_{equ}	17 µm X 45 µm	0.566 pF
	R_{bal}	5 µm X 60 µm	590.93 Ω

When using HBTs, ballast resistors are important since they prevent the device from drawing too much current and causing thermal runaway. From Fig. 3.7, V_s is fixed. So when the HBT starts to draw more current, the voltage across the resistor, V_{bal} will start to increase and this causes V_{be} to decrease. If V_{bal} keeps increasing, V_{be} will drop below the threshold voltage and the HBT will turn off. There are two ways in which ballasting can be performed. The resistors can be placed either in shunt (parallel ballasting) or in series (series ballasting) to the base terminal. For the design utilizing parallel ballasting, an additional resistor, R_{sta} is added in series to the base which acts as a stabilizing resistor. Another technique used to ballast the HBT is to use a resistor in the emitter but is not used in PAs because it lowers the gain and efficiency.

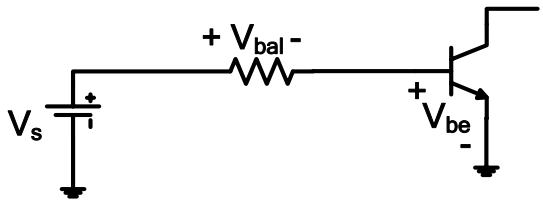

Figure 3.7: Function of a ballast resistor

So far, it has been assumed that the collector and base lines have equal characteristic impedance and phase velocities. However, this can only be achieved if C_{be} and C_{ce} are equal. However, in practice C_{ce} is much smaller than C_{be} and so steps must be taken to equalize the base and collector line phase velocities. One method is to add an additional capacitance, C_{equ} in series with C_{be} in order to reduce the input capacitance at the base-line and make it equivalent to C_{ce}. By using series capacitors, base line losses can also be reduced since it increases the base periphery of the devices. This results in an increased broadband output power performance.

3.2.4 MMIC Design

With ideal HBTs, the distributed amplifier can achieve more gain by employing more sections. However, in reality, the presence of parasitics in the HBT limits the maximum number of sections that can be usefully employed. The base and collector

line attenuation limits the number of devices in a distributed amplifier configuration. After a certain number of sections, the input signal becomes so weak that there is no benefit in adding more sections.

The MMIC die for DA1 to DA4 has four sections (four unit cells as shown in Section 3.2.3). Spiral inductors form both the collector and base line inductances. The WIN process allows the use of spiral or rectangular circular inductors. Spiral inductors are used since the have less current crowding at the corners compared to rectangular inductors resulting in less resistance. Figs. 3.8 and 3.9 both show the overall schematic for the MMIC DA. L_A and L_B represent the collector and base line inductances, respectively. The size of the first DA MMIC die is 2020 µm by 660 µm.

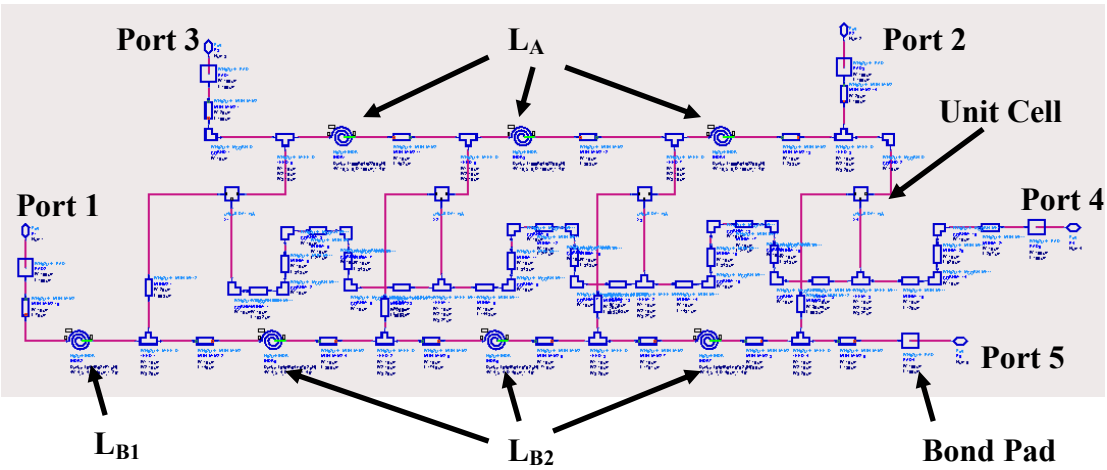

Figure 3.8: MMIC schematic for DA1 and DA2

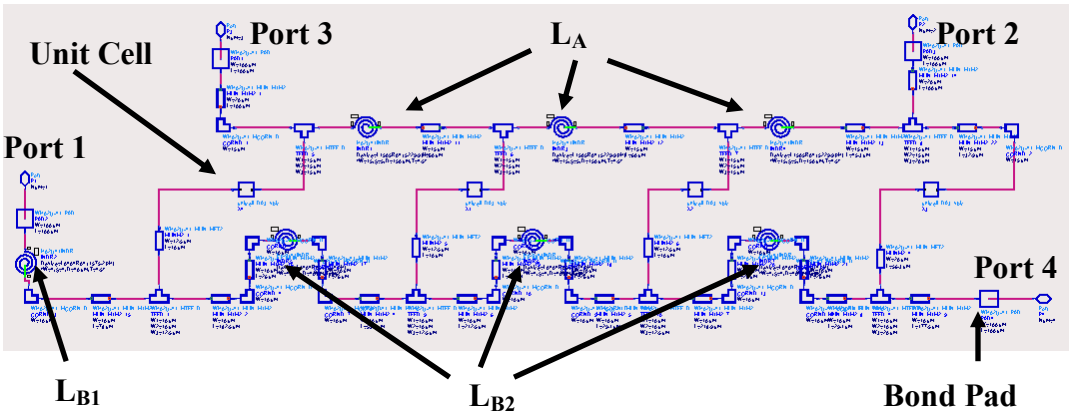

Figure 3.9: MMIC schematic for DA3 and DA4

Figs. 3.8 and 3.9 also show the interconnecting metal and 100 μm wide bond pads. These bond pads allow wirebonds to be connected to the MMIC for biasing and tuning purposes. The collector line is made up of Metal1 and Metal2. The maximum current density for Metal1 is 4 mA/μm and 8 mA/μm for Metal2. A combination of both gives a total current density of 12 mA/μm. The maximum I_C for each HBT is 32 mA. Assuming the peak current swing is up to 2/3 of the maximum, this means the I_C would be 22 mA. Therefore, with a total of 8 HBTs, the collector current can go up to 176 mA. The collector line is chosen to be 15 μm in width so that it can handle 180 mA (15 μm X 12 mA/μm). The base line is made out of Metal1 with a width of 10 μm, since base currents are usually very small.

Table 3.3 shows the component values indicated in Figs. 3.8 and 3.9.

Table 3.3: Component values for MMIC (First design iteration DA)

DA	**Component**	**Size**			**Inductance**
		Width	**Spacing**	**Turns**	
DA1 and DA2 (Parallel ballasting)	L_A	15 μm	5 μm	4	5229.9 pH
	L_{B1}	4 μm	4 μm	2	471 pH
	L_{B2}	4 μm	4 μm	4	1575.2 pH
DA3 and DA4 (Series ballasting)	L_A	15 μm	5 μm	4	5229.9 pH
	L_{B1}	4 μm	4 μm	4	1575.2 pH
	L_{B2}	4 μm	4 μm	6	3574 pH

The HBT diffusion capacitance is strongly dependant on the device collector current and dominates the input capacitance [116]. The input capacitance is expressed as

$$C_\pi = C_{diffusion} + C_{depletion} \tag{3.2}$$

The following equations are used to obtain $C_{diffusion}$ and $C_{depletion}$.

$$Q_{diffusion} = T_{FF} . \frac{I_F}{q_b} \tag{3.3}$$

$$T_{FF} = Tf\left[1 + Xtf\left(\frac{I_F}{I_F + Itf}\right)^2 .\exp(V_{bci}/(1.44Vtf))\right] \tag{3.4}$$

$$I_F = I_S\left(\exp(V_{bei}/N_f V_{th}) - 1\right) \tag{3.5}$$

$$I_R = I_S\left(\exp(V_{bci}/N_r V_{th}) - 1\right) \tag{3.6}$$

$$q_b = \frac{q_1}{2}\left(1 + \sqrt{1 + 4q_2}\right) \tag{3.7}$$

$$q_1 = \frac{1}{1 - \frac{V_{bei}}{Var} - \frac{V_{bci}}{Vaf}} \tag{3.8}$$

$$q_2 = \frac{I_F}{Ikf} + \frac{I_R}{Ikr} \tag{3.9}$$

$$C_{diffusion} = diff\,(Q_{diffusion}, V_{be}) \tag{3.10}$$

$$C_{depletion} = C_{je}\left(1 - \frac{V_{be}}{V_{je}}\right).\exp(-M_{je}) \tag{3.11}$$

A MATLAB program was written to calculate the values in Table 3.5 using equations (3.3) to (3.11) and the data in Table 3.4. The $C_{diffusion}$ and $C_{depletion}$ will be used in the nonlinear analysis of the HBT explained in Section 3.11.2

Table 3.4: Parameters obtained from Gummel Poon model [109]

Parameter	Description	Value
V_{be}	Voltage across base-emitter terminals	1.375 V
V_{be}	Voltage across base-collector terminals	-3.625 V
Tf	Ideal forward transit time	3 ps
Xtf	Excess transit time coefficient	0.6
Itf	Excess transit time dependence on I_F	1 mA
Vtf	Excess transit time dependence on V_{bc}	100 V
I_S	Saturation current	0.4293 yA
N_f	Forward ideality factor	1.006
N_r	Reverse ideality factor	1.002
V_{th}	Thermal voltage	26 mV
Vaf	Forward Early voltage	1000 V
Var	Reverse Early voltage	1000 V
Ikf	Forward base high current injection	1 A
Ikr	Reverse base high current injection	1 A
C_{je}	Zero bias base-emitter depletion capacitance	0.2081 pF
V_{je}	Base-emitter built in potential	3.2 V
M_{je}	Base-emitter junction grading coefficient	0.3

Table 3.5: Calculated parameters based on equation (3.3) to (3.11)

Parameter	Description	Value
I_F	Ideal forward collector-emitter current	0.0291 A
I_R	Ideal reverse emitter-collector current	0.4293 yA
q_1	Early voltage effect on base charge function	0.9978 C
q_2	Webster effect on base charge function	0.0291 C
q_b	Normalized base charge function	1.026 C
T_{FF}	Transit time constant for base-emitter junction	3 ps
$C_{diffusion}$	Base-emitter diffusion capacitance	3.2682 pF
$C_{depletion}$	Base-emitter depletion capacitance	0.2463 pF

3.2.5 Terminating Resistors and External Tuning Elements

The MMICs (explained in Section 3.2.4) are die-attached to testboards and are described in Section 3.4. Figs. 3.10 and 3.11 show the location of the external SMT components with their corresponding port and Table 3.6 shows the component values.

Table 3.6: Values for external SMT components (First design iteration DA)

DA	Component	Manufacturer Code	Value
DA1	L_{Ext1}	Murata LQG15HN3N9S02	3.9 nH
	L_{Ext2}	Murata LQG15HN2N7S02	2.7 nH
	R_{T1}	Vishay CRCW0402120RFKED	120 Ω
	R_{T2}	Vishay CRCW040245R3FKED	45 Ω
	C_{bypass}	Murata GRM21BR71C105KA01	1 μF
	DC block	Murata GRM1555C1H101JZ01	100 nF
DA2	L_{Ext1}	Murata LQG15HN3N3S02	3.3 nH
	L_{Ext2}	Murata LQG15HN2N7S02	2.7 nH
	R_{T1}	Vishay CRCW0402120RFKED	120 Ω
	R_{T2}	Vishay CRCW040245R3FKED	45 Ω
	C_{bypass}	Murata GRM21BR71C105KA01	1 μF
	DC block	Murata GRM1555C1H101JZ01	100 nF
DA3	L_{Ext1}	Murata LQG15HN3N3S02	3.3 nH
	L_{Ext2}	Murata LQG15HN3N9S02	3.9 nH
	R_{T1}	Vishay CRCW040257R6FKED	57 Ω
	C_{bypass}	Murata GRM21BR71C105KA01	1 μF
	DC block	Murata GRM1555C1H101JZ01	100 nF
DA4	L_{Ext1}	Murata LQG15HN2N2S02	2.2 nH
	L_{Ext2}	Murata LQG15HN3N7S02	3.9 nH
	R_{T1}	Vishay CRCW040227R4FKED	27 Ω
	C_{bypass}	Murata GRM21BR71C105KA01	1 μF
	DC block	Murata GRM1555C1H101JZ01	100 nF

Terminating resistors, R_{T1} and R_{T2} at the base line absorbs signals generated in the forward direction and prevents unwanted reflections. The terminating resistor also plays a key role in maintaining flat gain throughout the band of operation. The use of bond pads enables the MMIC to be connected to other external SMT tuning elements. DC blocks prevent DC signals from entering the MMIC. The R_o resistors (in red) are 0 Ω resistors placed to form connections on the testboard. The testboard was designed with many openings to provide extra degrees of freedom in tuning.

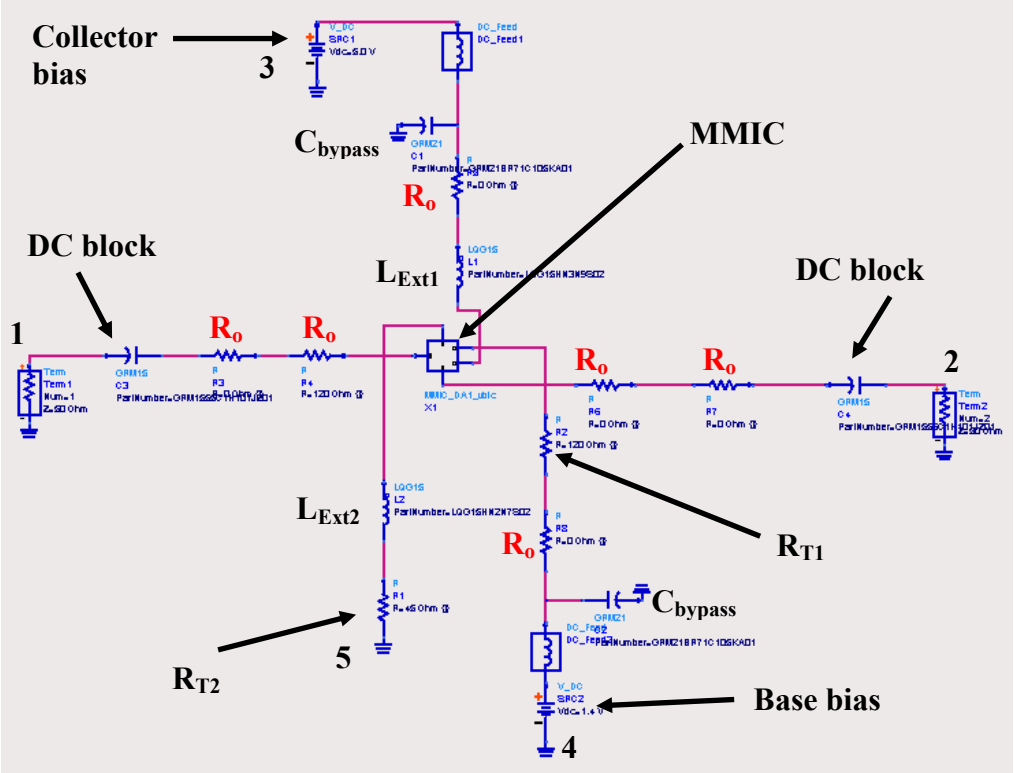

Figure 3.10: External tuning elements for DA1 and DA2

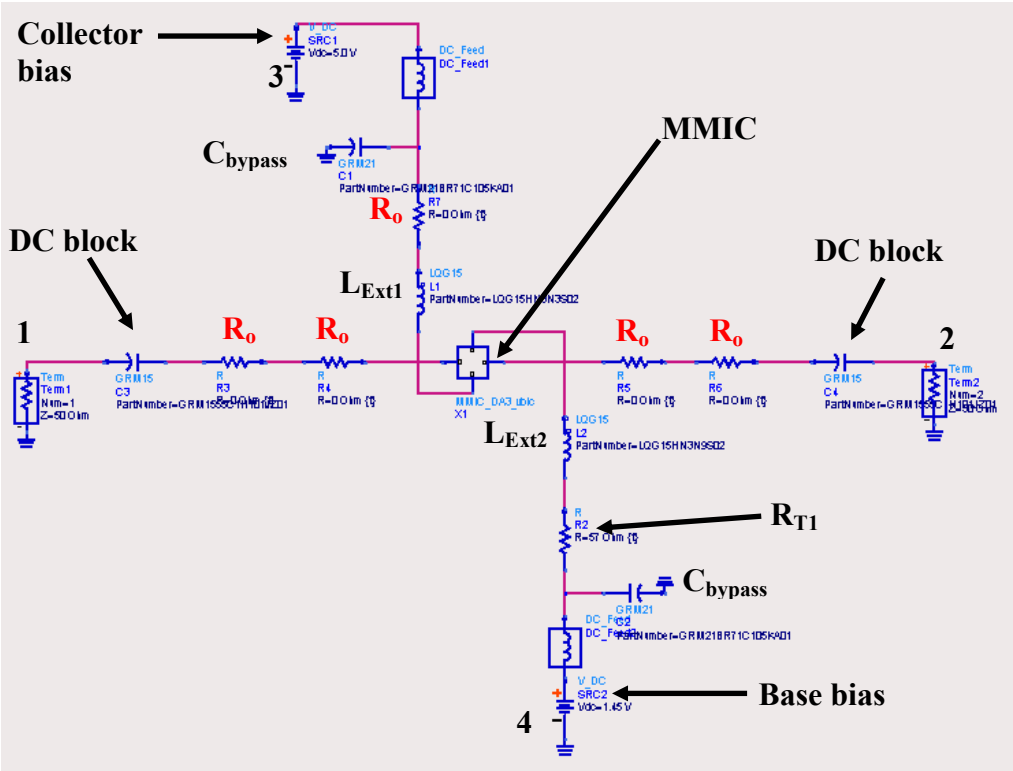

Figure 3.11: External tuning elements for DA3 and DA4

3.2.6 Location of LC trap at DA Output

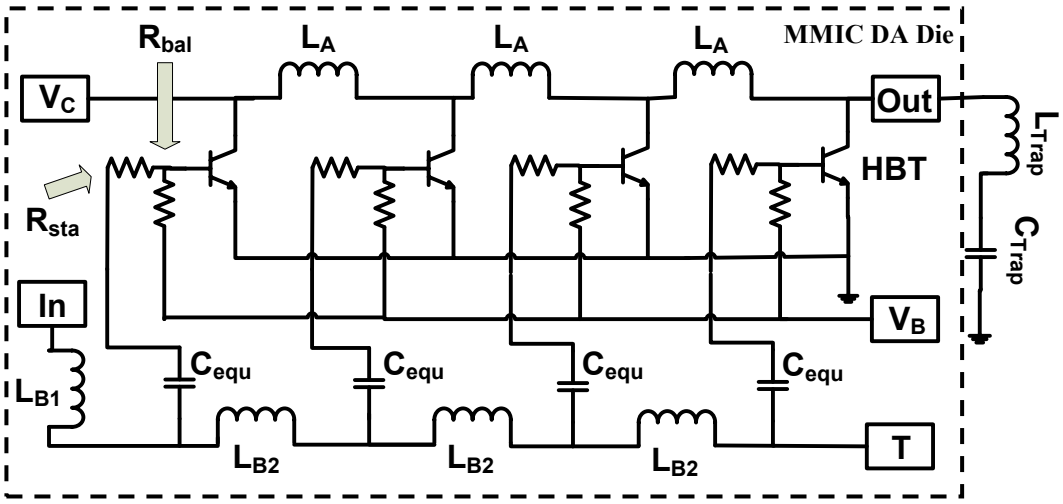

Figure 3.12: Location of output LC trap

As shown in Fig. 3.12, the improvement in linearization is achieved using a low impedance termination formed by a series inductor-capacitor network (LC trap), placed at the collector line which is the output of the MMIC. These traps are implemented externally through the use of 0402 (40 mils X 20 mils) SMT components. Table 3.7 lists the LC trap values and are chosen to form low impedance at the envelope frequency (ω_2–ω_1). The reason they have to be implemented externally is because it is very impractical to fit an inductor with a large value (e.g. 100 nH) onto the die. For instance, three 5.2 nH inductors (shown in MMIC layout, Fig. 3.12) take up nearly half of the die space.

Table 3.7: Component values for output LC trap

Component	Manufacturer Code	Value
L_{trap}	Murata LQW18ANR10G00	100 nH
C_{trap}	Murata GRM155R71H222KA01	2.2 nF
	Murata GRM155R71H242KA01	2.4 nF
	Murata GRM155R71H272KA01	2.7 nF

3.3 Layout for First Design Iteration DA

Utilizing the design kit provided by WIN, circuit layouts of the MMIC DA were performed using ADS. This is an important step in the fabrication of the die since it translates the schematic design into a layout arrangement of the actual MMIC. Fig. 3.13 (a) shows the unit cell (or section) for DA1 and DA2 which uses parallel ballasting resistors. Fig. 3.13 (b) shows the unit cell for DA3 and DA4 which uses series ballasting resistors. The resistors are implemented as Thin Film Resistors (TFR) with a sheet resistance of 50 Ω/square. The capacitors used are Metal – Insulation – Metal (MIM) in which is a flat parallel plate structure with a very thin insulator to maximize the capacitance between the plates. As described earlier, the HBT used is the RQ1A202F2_M2 transistor. Backvias are connected to both sides of the emitter terminals to form a path through the GaAs substrate to ground.

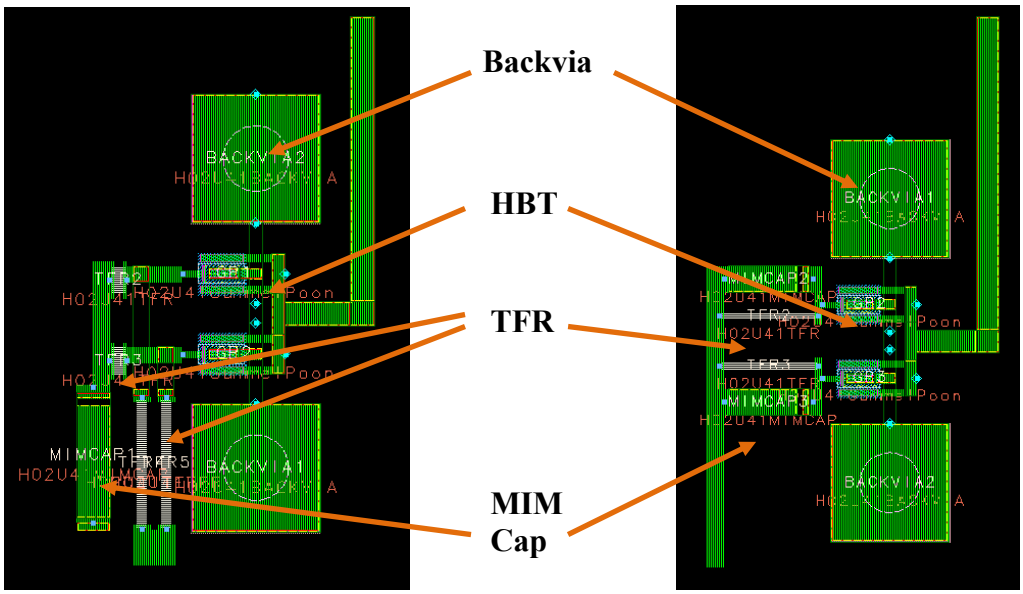

Figure 3.13: (a) Layout of unit cell for DA1 and DA2 (left)

(b) Layout of unit cell for DA3 and DA4 (right)

The dimensions for the die are 2020 µm X 660 µm. Figs. 3.14 and 3.16 show the layout for DA2 and DA4, respectively. Figs. 3.15 and 3.17 show the microphotograph of the actual MMIC after they have been fabricated. From Figs. 3.14 and 3.16, it is shown how the unit cells are cascaded to form sections of the DA. Spiral inductors form the collector and base transmission line inductances.

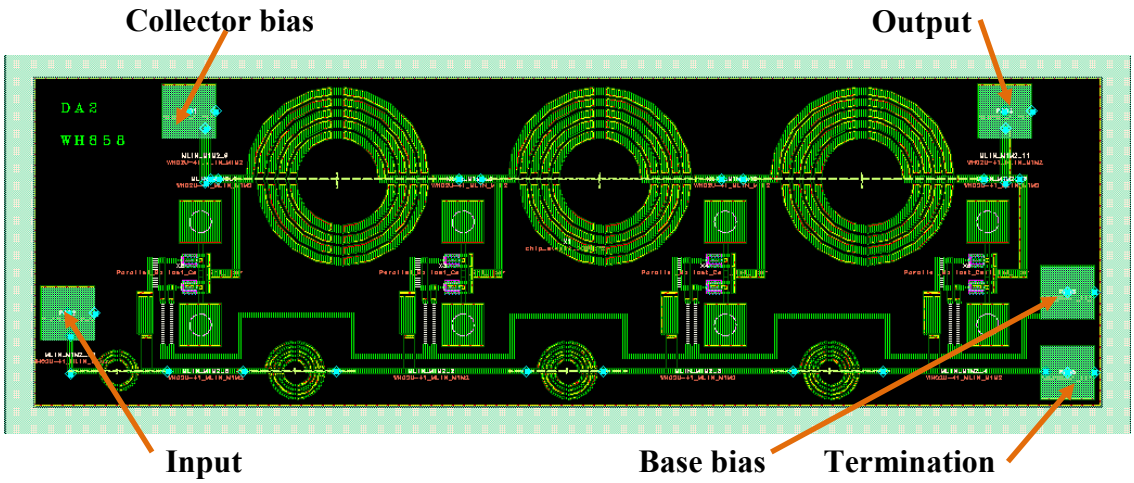

Figure 3.14: Layout for DA2

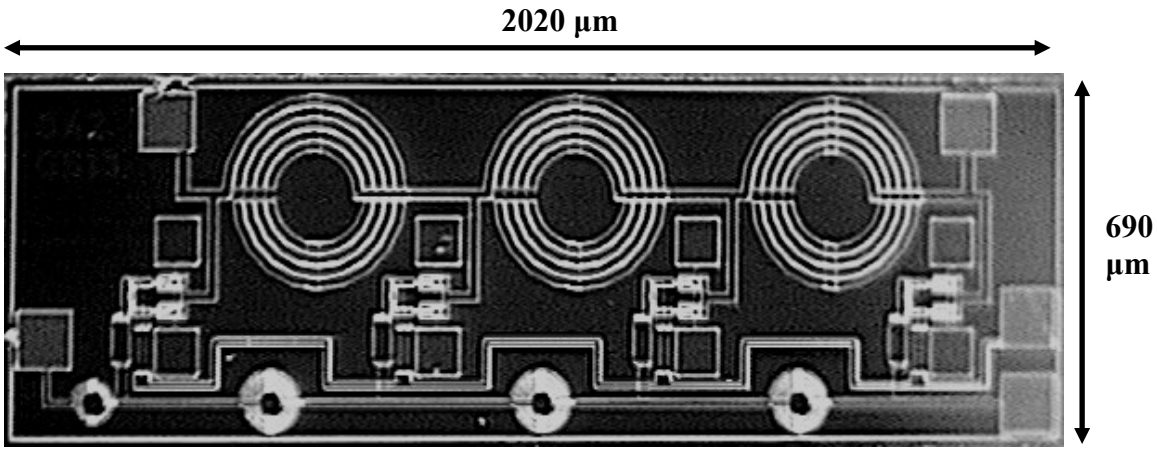

Figure 3.15: Microphotograph for DA2

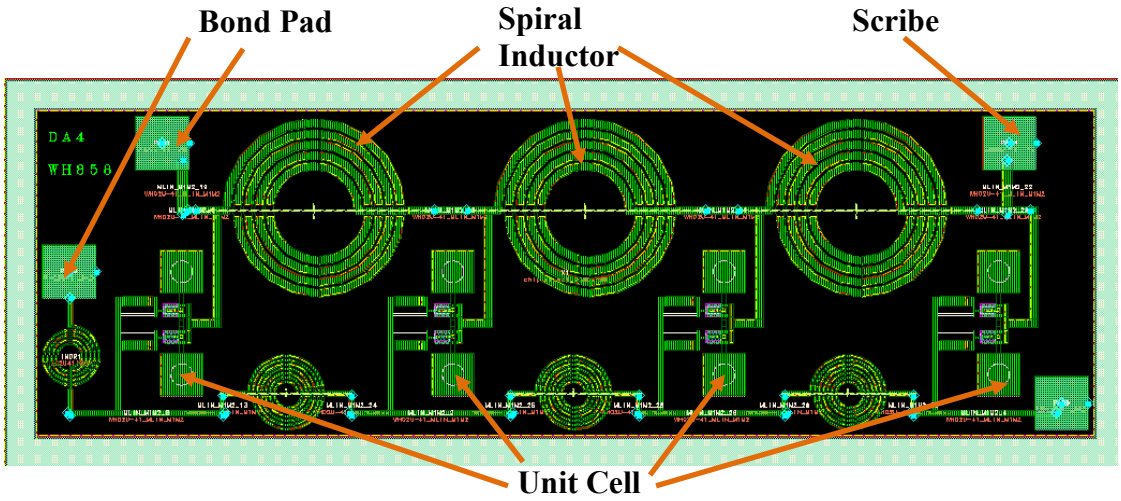

Figure 3.16: Layout for DA4

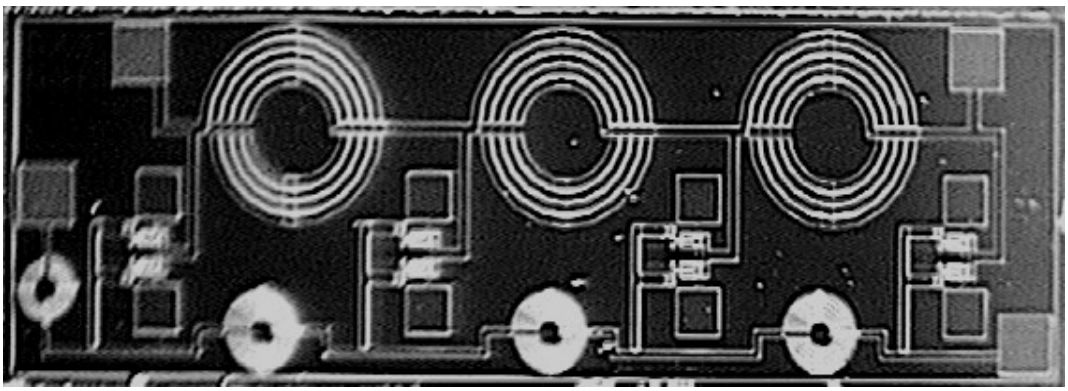

Figure 3.17: Microphotograph of DA4

Square bond pads with length 100 μm are placed on the periphery of the MMIC to supply the bias currents, input and output signals. Outer bond pads are placed at the corners and with sufficient separation to prevent the bond wires from touching and shorting out. Fig. 3.14 identifies the function of each bond pad. The input signal comes in from the left and connects to the base of the HBTs. This excites each HBT and produces a current on the collector line which is connected to the output bond pad on the right of the MMIC.

There are several rules to follow when performing the layouts. The major rules are [117]:

i. Minimum spacing between any pattern and the front side scribe lanes is 10 μm. As shown in Figs. 3.14 and 3.16, any layer (including bond pad) is separated from the scribe by at least 10 μm.
ii. Aspect ratio of chip dimension cannot exceed 3:1. Minimum chip area is 360 μm^2. The dimension for the first design iteration of the DA is 2020 μm X 660 μm. (It cannot be larger since it will exceed the maximum aspect ratio).
iii. No donut patterns are allowed for any metal layers and TFR.

Placing a minimum spacing of 10 μm between any pattern and the front scribe ensures that components on the MMIC do not get damaged when the saw cuts the entire reticle into each individual die. The maximum aspect ratio of 3:1 ensures that the MMIC does not break in two since it is very fragile. Donut patterns are not allowed for the metal layers and TFR so that the chemical that performs the etching flows out and does not pool on the die. After the layouts have been completed, they are sent for Design Rule Check (DRC). DRC determines whether the physical layout of a particular chip satisfies recommended parameters known as Design Rules (such as the spacing between layers or the minimum width of the layers). If these rules are violated, the design may not function. Layout Versus Schematic (LVS) checks are also required to ensure no errors were made in the connections. A short or open circuit at any point of the MMIC could “spell doom” because the DA will probably not function properly.

3.4 Testboard for First Design Iteration DA

In order to measure the MMIC DA and to provide external tuning, a testboard has been designed using AutoCAD. The testboard (or commonly known as prototype boards) use grounded co-planar waveguide (GCPW) instead of microstrip as its transmission media. CPW was introduced in 1969 and supports a quasi-TEM mode of propagation with the active metallization and the ground plane on the same side of the substrate [118].

A CPW has a centre conductor placed symmetrically between ground planes. Though inhomogenous like the microstrip, it is less dispersive and the ground planes are readily accessible. CPW is also open to hybrid elements or tuning, making it suitable for the testboard. The characteristic impedance of the CPW depends on the ratio of the strip width to the ground plane spacing. In conventional CPW, the ground plane extends indefinitely, but in grounded CPW (GCPW), the extent of the grounds is limited and results in reduced coupling of adjacent and crossing CPW lines. The structures for microstrip and grounded coplanar waveguide are shown in Fig. 3.18.

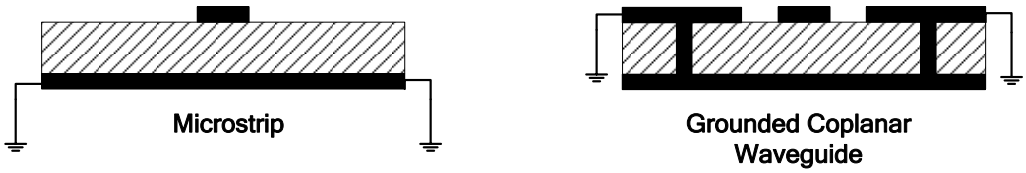

Figure 3.18: Microstrip and grounded co-planar waveguide transmission lines

The GCPW is selected for the testboard and by using Agilent's AppCAD, the strip width and spacing for the ground planes can be selected to yield 50 Ω. The screenshot of the calculation is shown in Fig. 3.19.

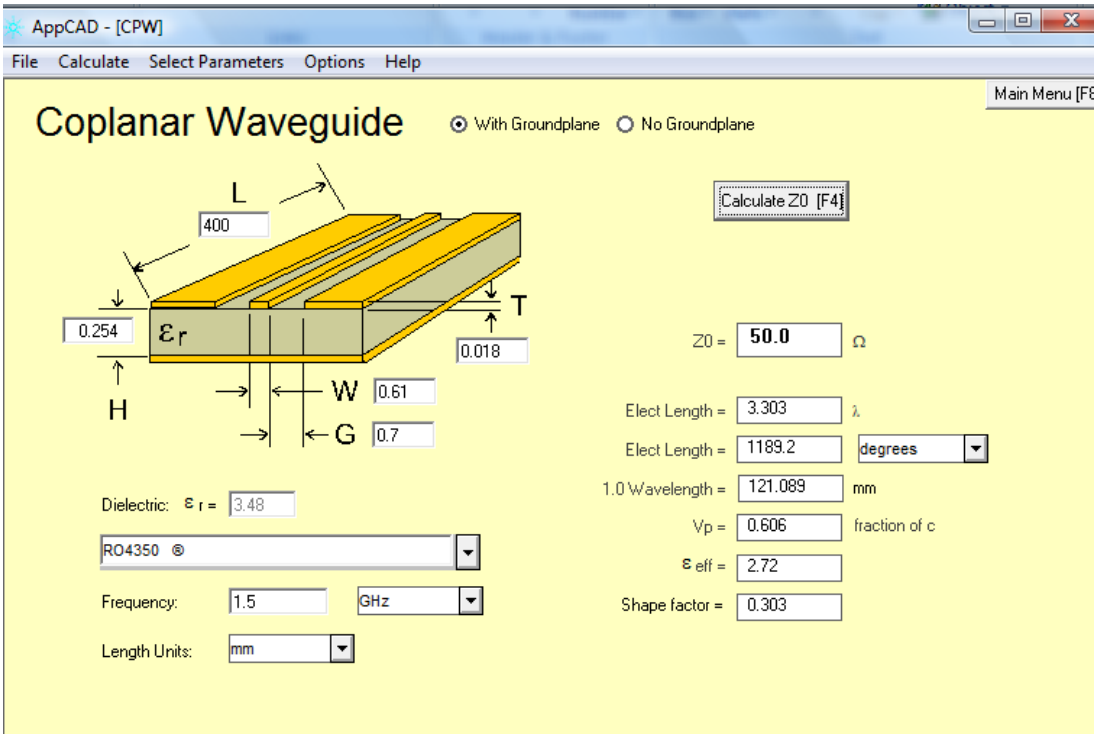

Figure 3.19: Screenshot of AppCAD for testboard design

As shown, the strip width must be 0.61 mm and the spacing 0.7 mm for the impedance to be 50 Ω. The dielectric used is Rogers 4350 with a height of 0.254 mm (10 mils) and dielectric constant of 3.48. Thickness of the metal is 0.018 mm.

The layout of the first testboard (Testboard_1) is shown in Fig. 3.20. This diagram includes all the design layers and shows the location of the input and output lines with the MMIC at the centre of the testboard. The circles around the layout are plated-through vias which connect to the inner metal (ground). The finishing is soft gold (immersion gold) so that wire bonding can be made. Hard gold finishing makes it difficult for wirebonding. The total length and width of the testboard is 40 mm X 50 mm. The testboard has 3 metal layers and the cross section is described in Fig. 3.21. Table 3.8 shows a description of all the design layers for the testboard.

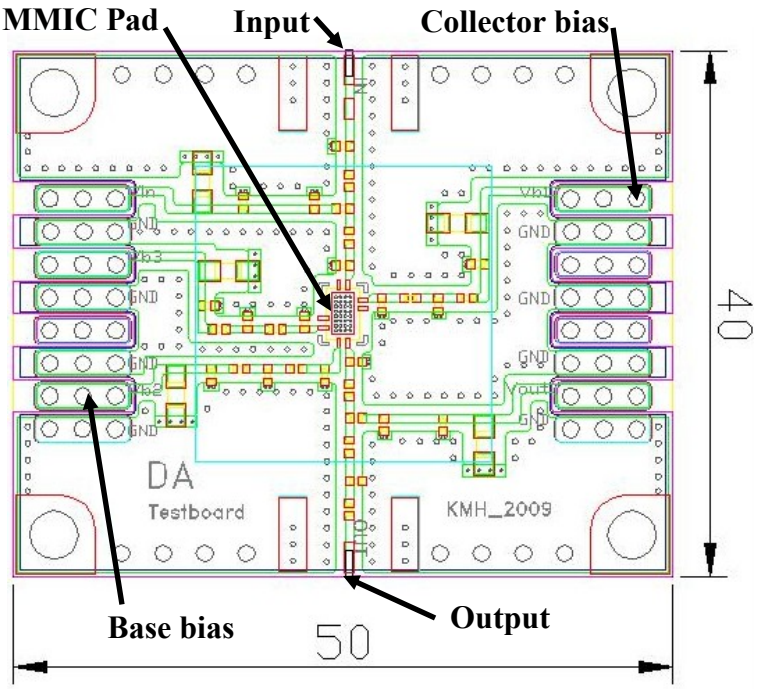

Figure 3.20: Layout of Testboard_1

0.5 OZ CU ========== LAYER 1: TOP METAL
0.010” ROGERS 4350 (DIELECTRIC)
0.5 OZ CU ========== LAYER 2: INNER METAL
0.052” FR4 (SUPPORT MATERIAL)
0.5 OZ CU ========== LAYER 3: BACK METAL

Figure 3.21: Layer Cross Section for testboard

Table 3.8: Layers for testboard

Layer	Description
Top silk	Printing for text
Vias PT	Plated through hole vias
Top Metal	Top side copper
Solder Mask Top	Top layer solder mask (negative mask)
Inner Metal	Inner metal layer (Ground)
Back Metal	Bottom side copper
Solder Mask Bottom	Bottom layer solder mask (negative mask)

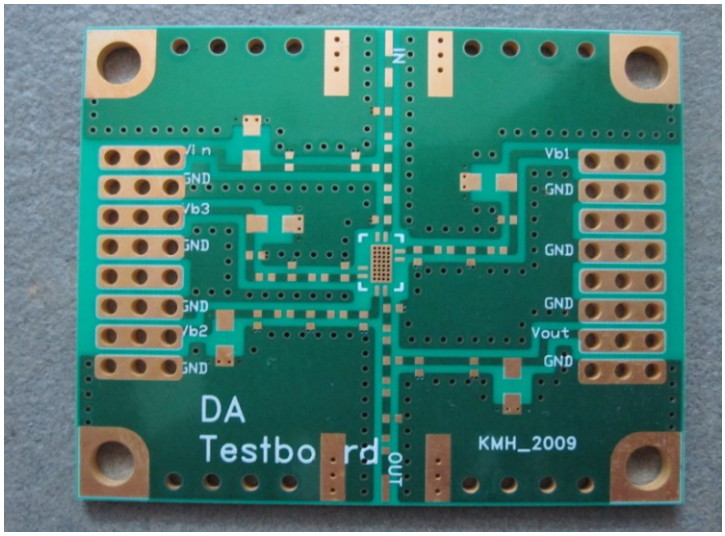

Figure 3.22: Front view of Testboard_1

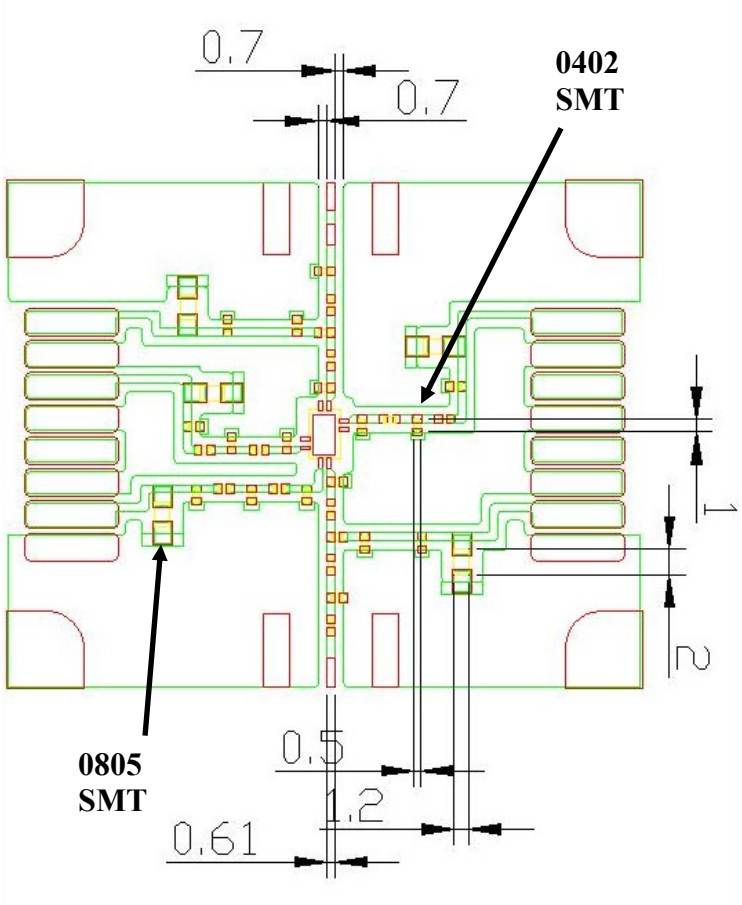

Figure 3.23: Layout of Testboard_1 with top metal and top solder mask layers

The finished product of Testboard_1 is shown in Fig. 3.22. Fig. 3.23 shows the layout with only the top metal layer (in green) and the top solder mask (in pink). The solder mask layer is a negative layer which exposes the metal layer beneath it. This is to enable SMT components to be soldered to the testboard. Comparing Figs. 3.22 and 3.23, it is clear that areas with the pink layer have exposed metal. From Fig. 3.23, the dimensions for the metal line follow the calculations made in Fig. 3.19 to ensure the transmission line is matched to 50 Ω. Openings for 0402 (40 mils X 20 mils) and 0805 (80 mils X 50 mils components are shown. The dimensions are in terms of mm so 40 mils ~ 1mm, 20 mils ~ 0.5 mm, 80 mils ~ 2mm and 50 mils ~ 1.2 mm.

Fig. 3.24 is a photo of the back view for Testboard_1. It can be compared with Fig. 3.25 which is the layout for the bottom metal layer (in purple) and bottom solder mask (in blue). The measurements comply with the pitch for SMA connectors which were used to provide the signals and bias currents. There is a large exposure at the bottom metal to act as a thermal opening in order to dissipate heat from the testboard.

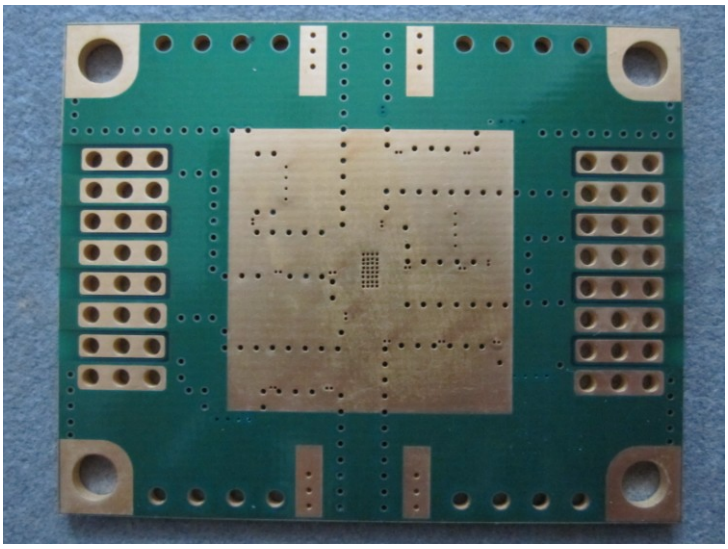

Figure 3.24: Back view of Testboard_1

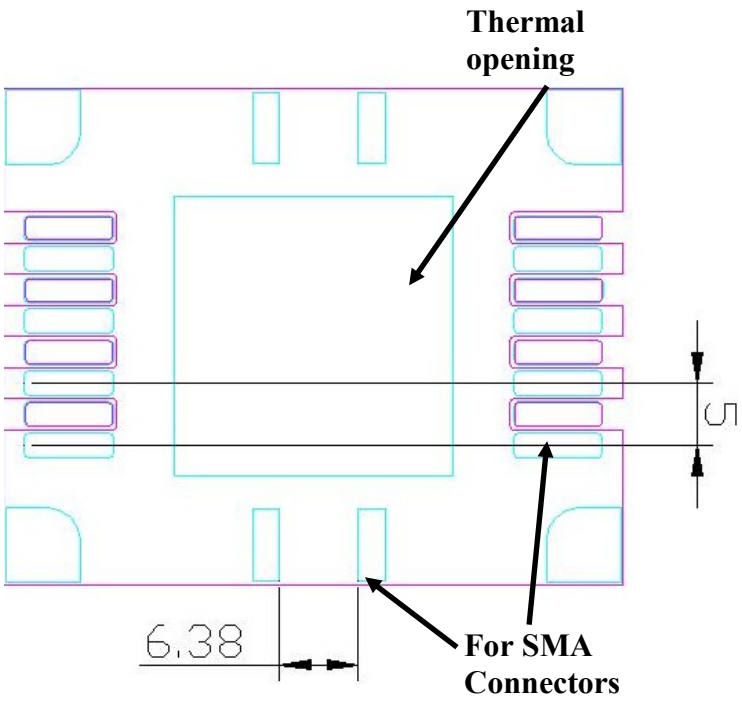

Figure 3.25: Layout of Testboard_1 with bottom metal and bottom solder mask layers

3.5 Second Design Iteration of Distributed Amplifier

For the second design iteration, the MMIC are fabricated using the WIN Semiconductor Corporation's H02U-43 InGaP/GaAs HBT foundry process [119]. In order to measure the effects of placing the low impedance termination at the input of the DA, a second DA design run must be made. This is because each unit cell in the first design has a C_{equ} capacitor which equalizes the phase between the base and collector lines. However, this capacitor is very small in value (~ 1 pF). Therefore, in order to provide a short circuit at the envelope frequency, a very large inductor is needed (1 mH). This forces the quality factor, Q to rise to an extremely high value. Q is given by:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{3.12}$$

With a typical LC trap value of 100 nH and 2.2 nF, the Q is only about 6/R. But with 1 mH and 1 pF components, the Q will rise to 31600/R. This is an increase by a factor of about 5200 and such a high Q makes the LC trap very selective and can only provide low impedance at an extremely narrow band. Furthermore, it is very difficult to find a 1 mH SMT inductor. The active devices as well as the base and collector bias voltages for the second design iteration are the same as the first.

3.5.1 Unit Cells

As mentioned earlier, the C_{equ} poses a problem to implement the LC trap at the input of the HBT. Therefore, this second design solves this problem by placing bond pads that bypass the capacitor and into the base of the HBT. This is shown in Figs. 3.26 to 3.32 for DA1A, DA1B and DA4A. The additional port which connects to the bond pad is shown in red. Basically, the unit cells for the second design are the same as the first. The difference is the addition of the extra port to the base of the HBT. Therefore, component values for the unit cells remain the same. The design measures taken for this unit cell have already been explained in Section 3.2.3.

DA1A and DA1B both uses parallel ballasting but they differ in the location of the port. For DA1A, the port goes directly to the base of the HBT, after the C_{equ} and R_{sta}. For DA1B, the port is in between C_{equ} and R_{sta}. In other words, the LC trap sees the R_{sta} impedance as well. DA4A uses series ballasting, therefore there is no R_{sta}. Table 3.9 lists the component values for the unit cells.

Table 3.9: Component values for unit cells (Second design iteration DA)

DA	Component	Size (Width X Length)	Value
DA1A and DA1B (Parallel ballasting)	C_{equ}	20 µm X 68 µm	0.966 pF
	R_{sta}	17 µm X 5 µm	14.06 Ω
	R_{bal}	6 µm X 75 µm	615.57 Ω
DA4A (Series ballasting)	C_{equ}	17 µm X 45 µm	0.566 pF
	R_{bal}	5 µm X 60 µm	590.93 Ω

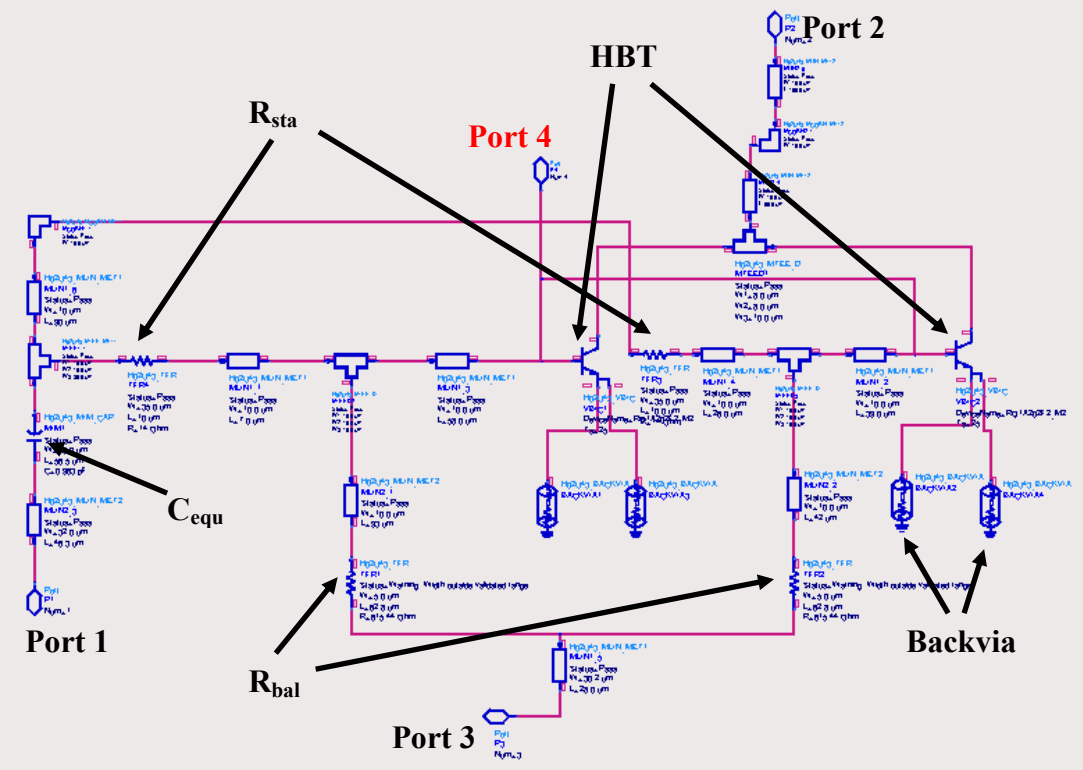

Figure 3.26: Unit cell for DA1A

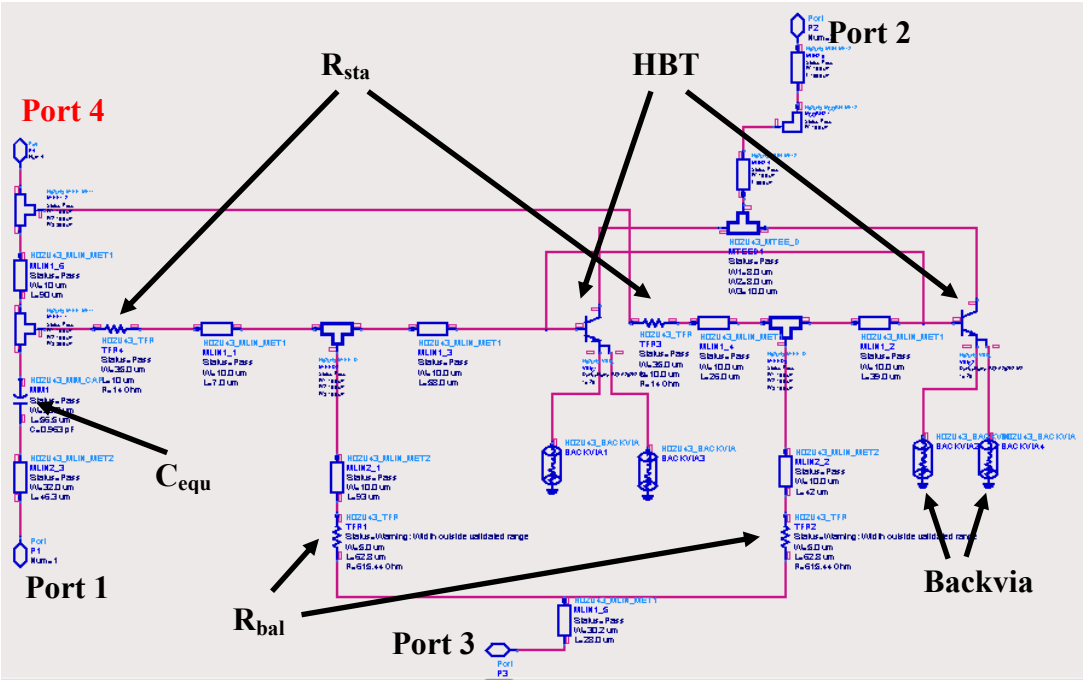

Figure 3.27: Unit cell for DA1B

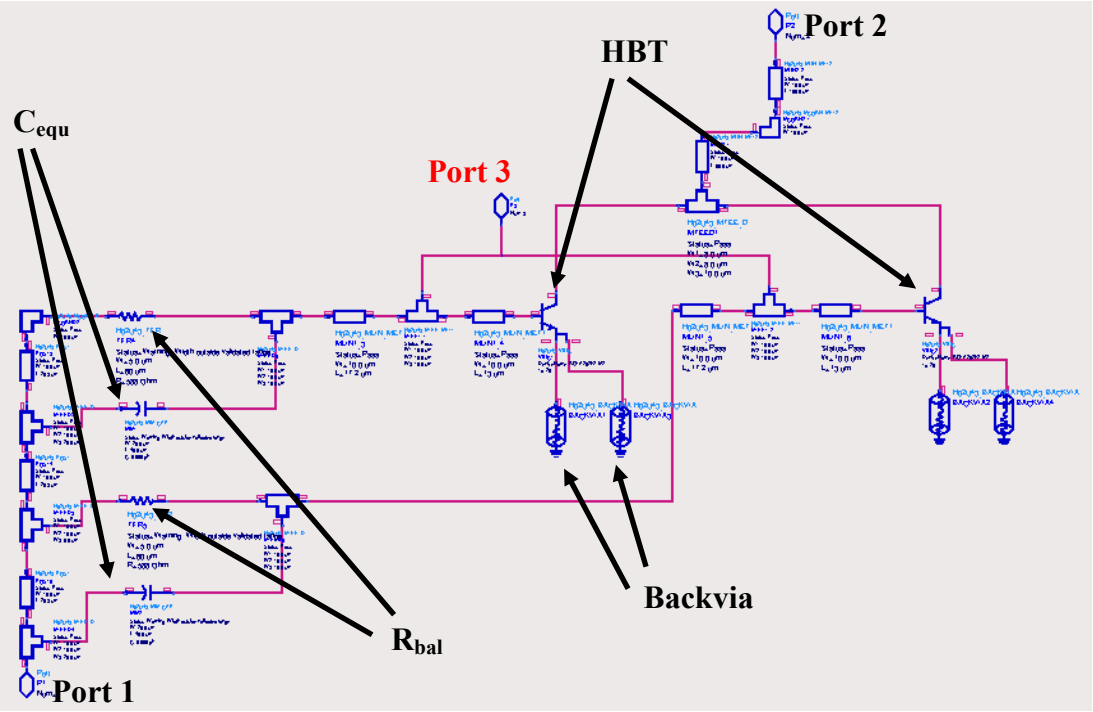

Figure 3.28: Unit cell for DA4A

3.5.2 MMIC Design

The second DA design uses the same inductor values as the first design. However, due to a space limitation in the reticle, the die size had to be reduced, forcing the MMIC to have only three stages. The inductor values are listed in Table 3.10.

Table 3.10: Component values for MMIC (Second design iteration DA)

DA	Component	Size			Value
		Width	Spacing	Turns	
DA1A and DA1B (Parallel ballasting)	L_A	15 µm	5 µm	4	5229.9 pH
	L_{B1}	4 µm	4 µm	2	471 pH
	L_{B2}	4 µm	4 µm	4	1575.2 pH
DA4 (Series ballasting)	L_A	15 µm	5 µm	4	5229.9 pH
	L_{B1}	4 µm	4 µm	4	1575.2 pH
	L_{B2}	4 µm	4 µm	6	3574 pH

The bond pads have also been shrunk to 75 μm^2 to save space. The dimensions of the second DA design are 1620 µm X 660 µm. Since there are three stages, each with its own additional bond pad for connection to the LC trap, there are three additional ports (indicated in red) for the MMIC as shown in Figs. 3.29 and 3.30.

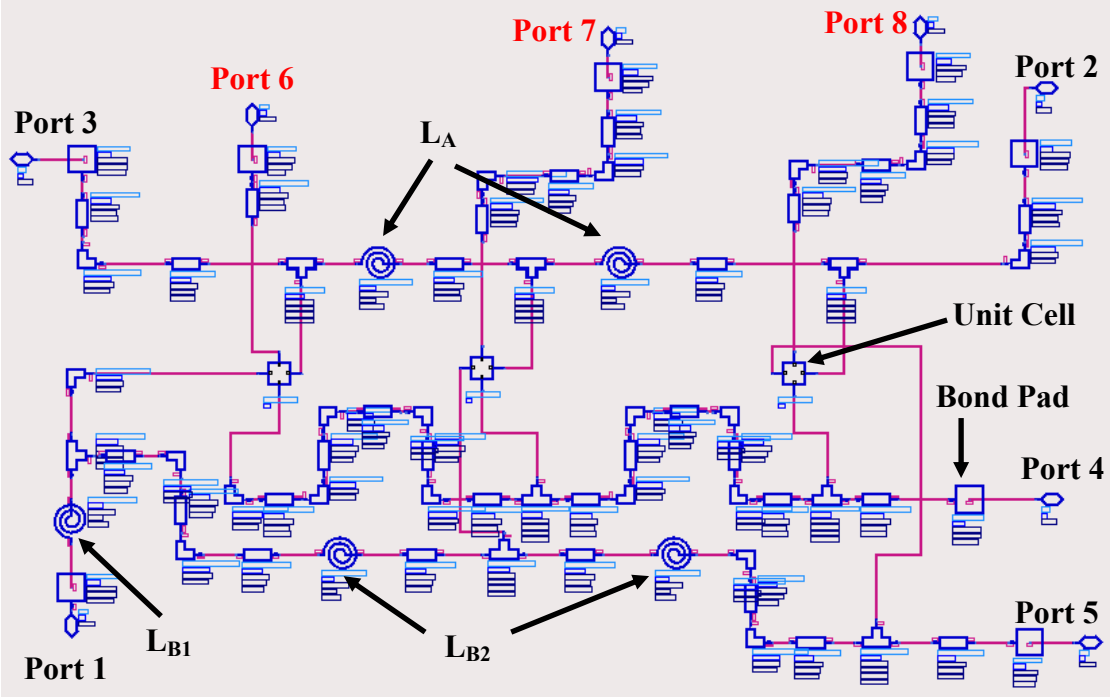

Figure 3.29: MMIC schematic for DA1A and DA1B

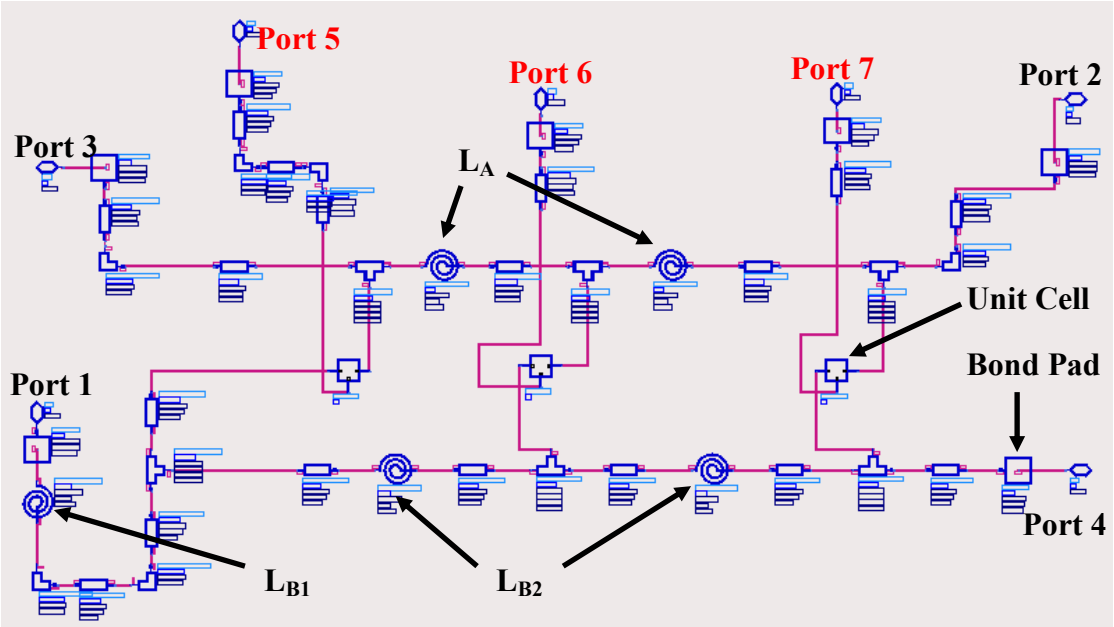

Figure 3.30: MMIC schematic for DA4A

3.5.3 Terminating Resistor and External Tuning Elements

Since the number of stages has been reduced, the terminating resistor and other external tuning elements are not the same as the previous design. They need to be readjusted to still meet the same specifications. The locations of the external SMT components are shown in Figs. 3.31 and 3.32 and Table 3.11 lists out their values.

Table 3.11: Values for external SMT components (Second design iteration DA)

DA	Component	Manufacturer Code	Value
DA1A and DA1B	L_{Ext1}	Murata LQG15HN1N8S02	1.8 nH
	R_{T1}	Vishay CRCW040239R3FKED	39 Ω
	C_{bypass}	Murata GRM21BR71C105KA01	1 µF
	DC block	Murata GRM1555C1H101JZ01	100 nF
DA4	R_{T1}	Vishay CRCW040222R4FKED	22 Ω
	C_{bypass}	Murata GRM21BR71C105KA01	1 µF
	DC block	Murata GRM1555C1H101JZ01	100 nF

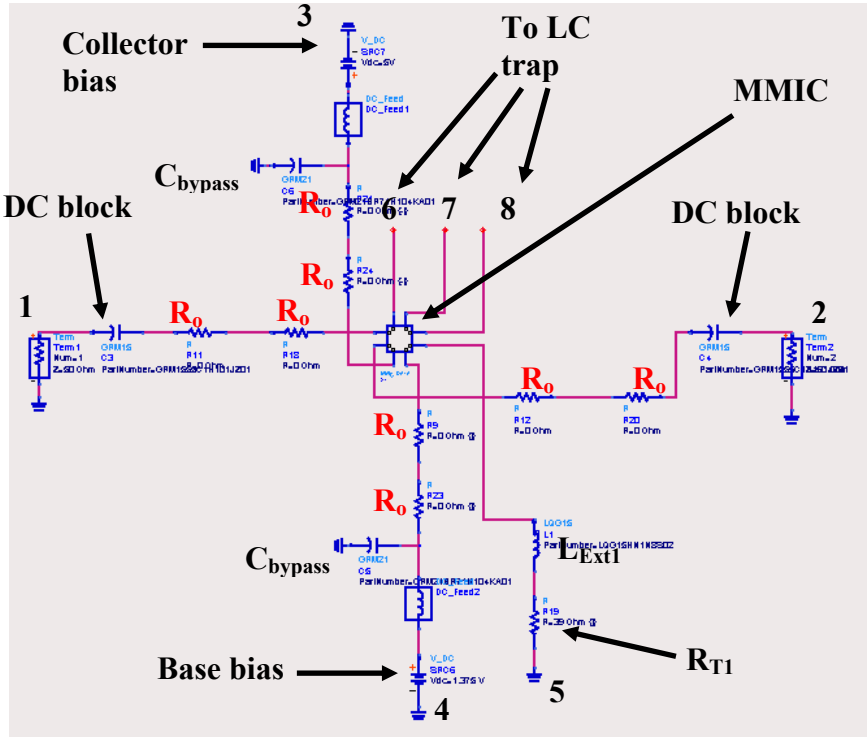

Figure 3.31: External tuning elements for DA1A and DA1B

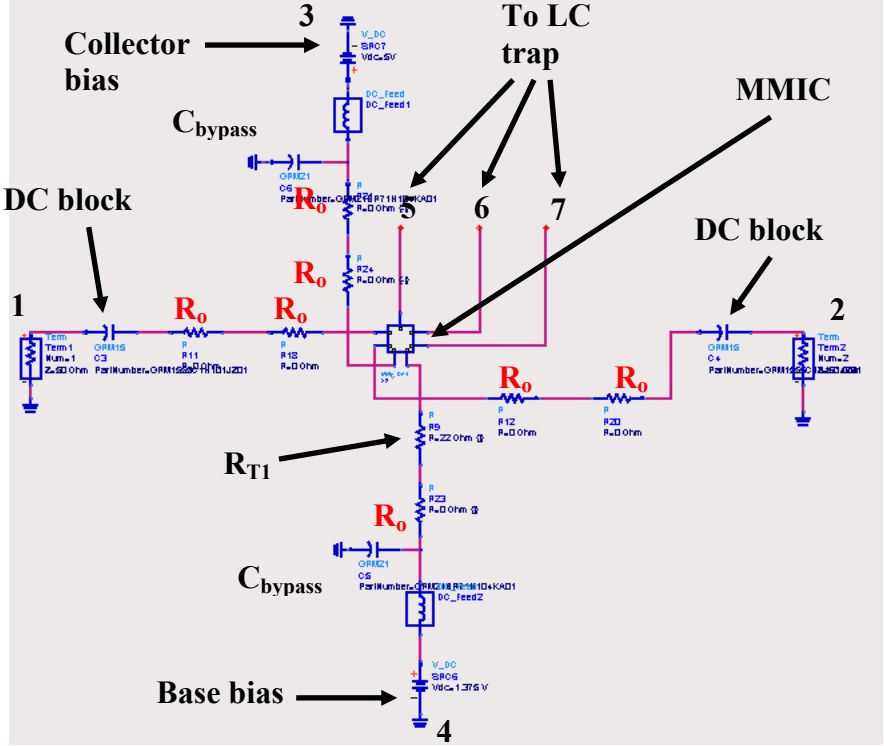

Figure 3.32: External tuning elements for DA4A

3.5.4 Location of LC trap at DA Input

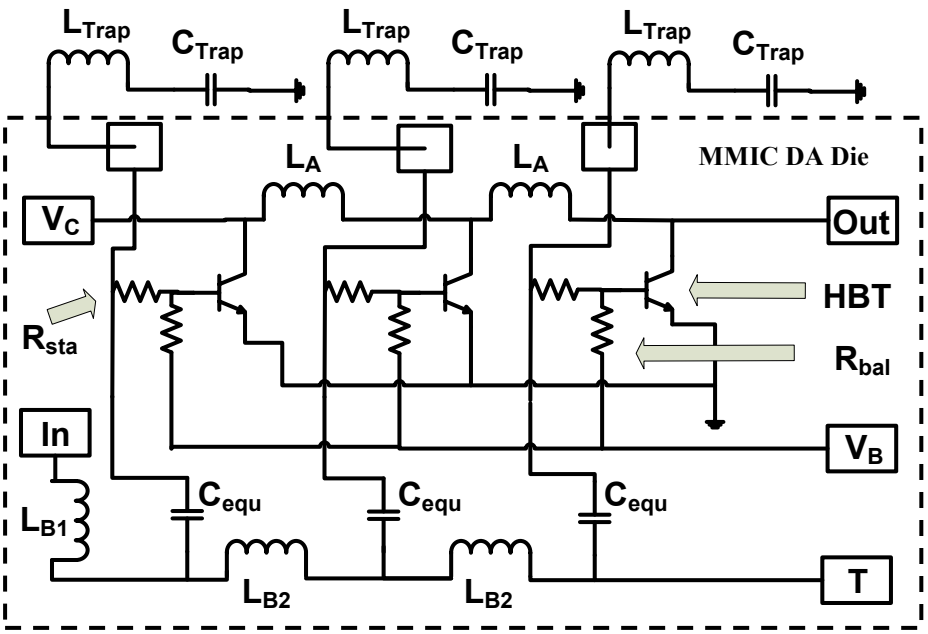

Figure 3.33: Location of input LC trap

As shown in Fig. 3.33, the LC trap is placed at the base, which is the input to the HBT. These traps are implemented externally through the use of 0402 (40 mils X 20 mils) SMT components. The inductor values have to be large so that it does not interfere with the in-band response of the DA [9]. Table 3.12 states the LC trap values and are chosen to form low impedance at the envelope frequency ($\omega_2 - \omega_1$).

Table 3.12: Component values for input LC trap

Component	Manufacturer Code	Value
L_{trap}	Murata LQW18AN68NG00	68 nH
	Murata LQW18AN82NG00	82 nH
	Murata LQW18ANR10G00	100 nH
	Murata LQW18ANR12G00	120 nH
C_{trap}	Murata GRM155R71H102KA01	1 nF
	Murata GRM155R71H222KA01	2.2 nF
	Murata GRM155R71H272KA01	2.7 nF
	Murata GRM155R71E472KA01	4.7 nF

3.6 Layout for Second Design Iteration DA

Figs. 3.34, 3.36 and 3.38 shows the layout for DA1A, DA1B and DA4A respectively. The connections to each bond pad are also shown. The layouts are the same as the first design with the exception of additional bond pads which connect to the base of the HBTs. The number of stages also had to be reduced from four to three because of the space limitation in the second design's reticle. The die size is now 1620 μm X 660 μm. The microphotographs of the MMIC DAs after fabrication are shown in Figs. 3.35, 3.37 and 3.39.

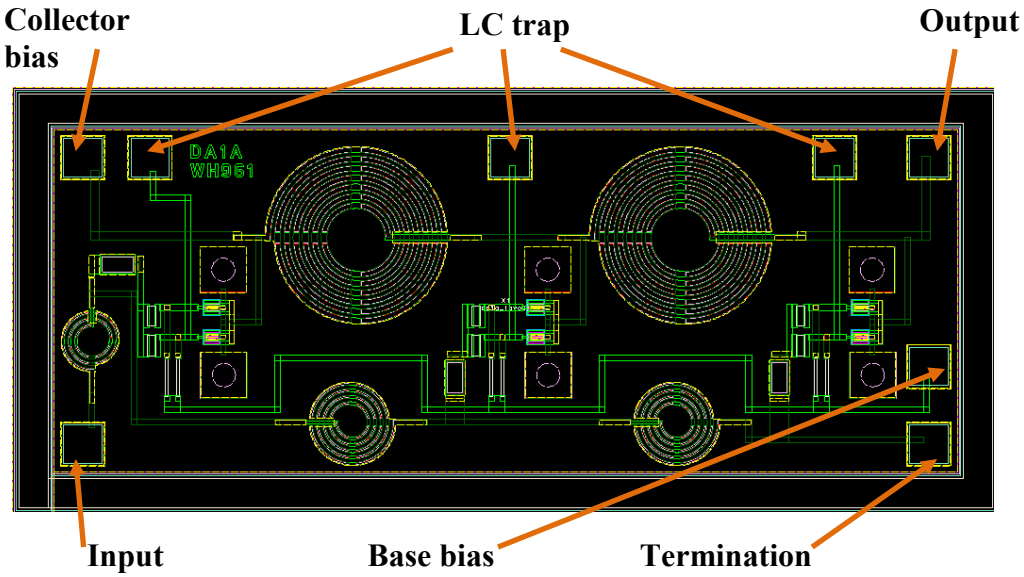

Figure 3.34: Layout for DA1A

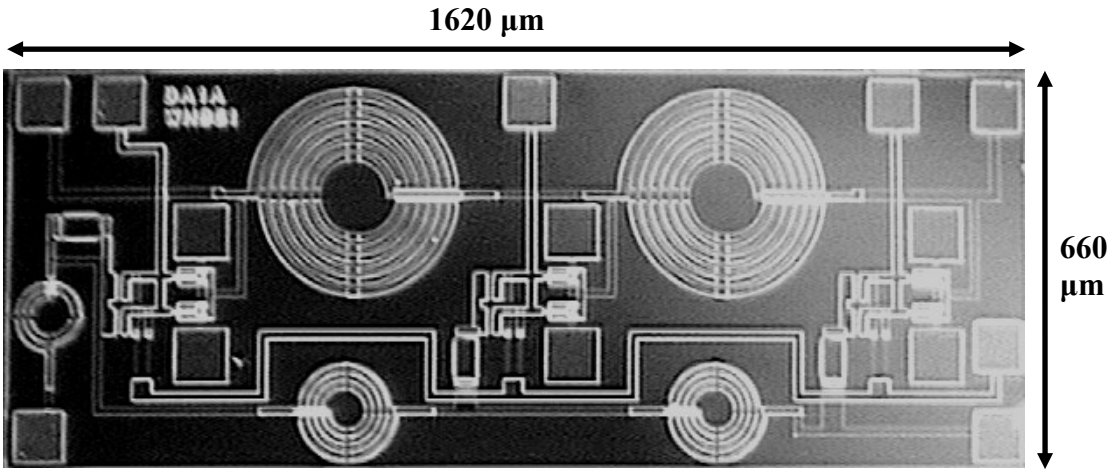

Figure 3.35: Microphotograph for DA1A

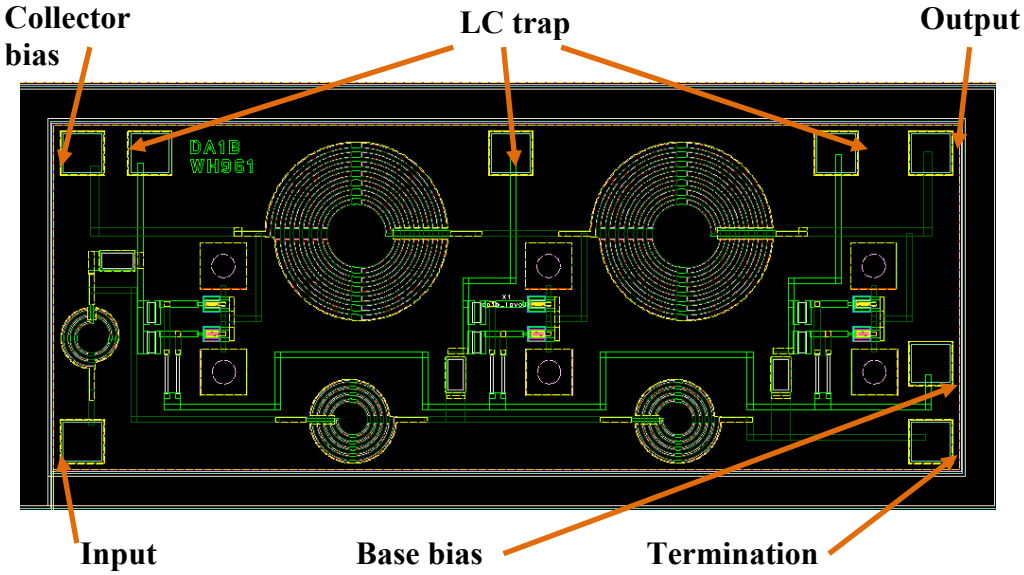

Figure 3.36: Layout for DA1B

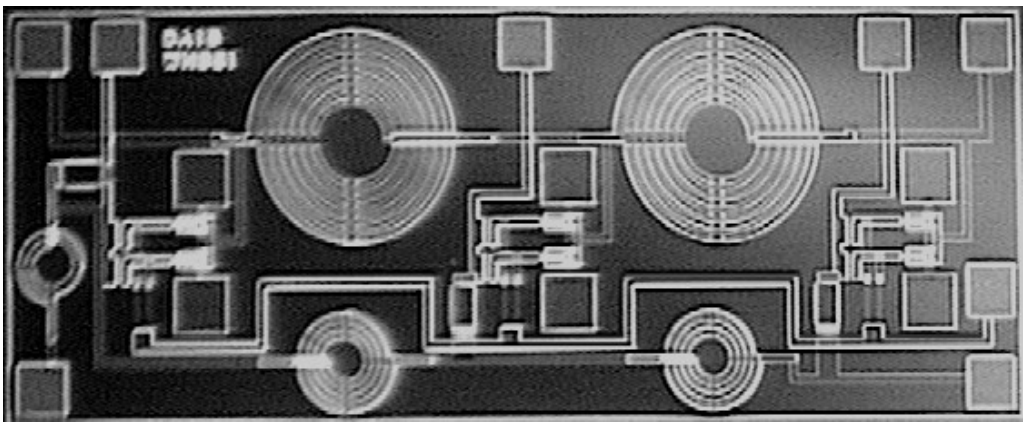

Figure 3.37: Microphotograph for DA1B

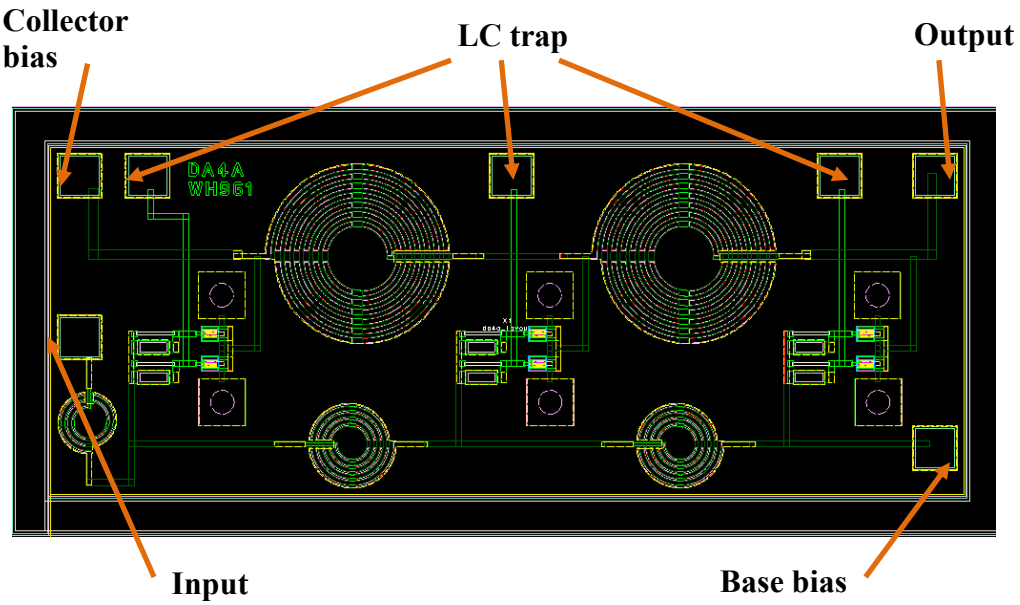

Figure 3.38: Layout for DA4A

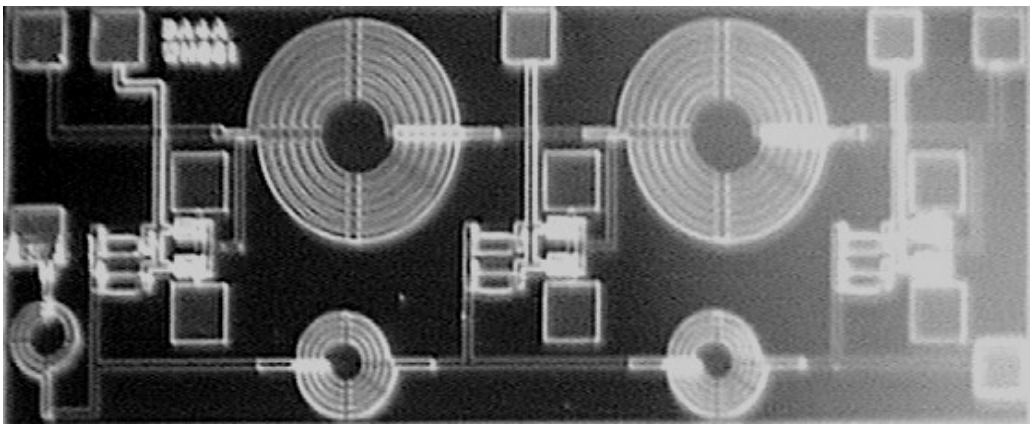

Figure 3.39: Microphotograph for DA4A

3.7 Testboard for Second Design Iteration DA

Fig. 3.40 shows the layout of Testboard_2 whereas Fig. 3.41 is a photograph of the board once it has been fabricated. The layout for Testboard_2 with only the top metal and top solder mask layers is in Fig. 3.42. The second testboard design still uses the same signal line width (0.61 mm) and gap (0.7 mm) to give 50 Ω of characteristic

impedance as well as the same board dimension (40 mm X 50 mm). The layers for this board are the same as the first design and the design methodology has already explained in Section 3.4. The main difference between the two boards is the additional runners in Testboard_2 to accommodate the input LC traps. The size of the MMIC pad was also reduced since the die size for the second DA design is smaller. A comparison between the first and second testboard design is shown in Fig. 3.42.

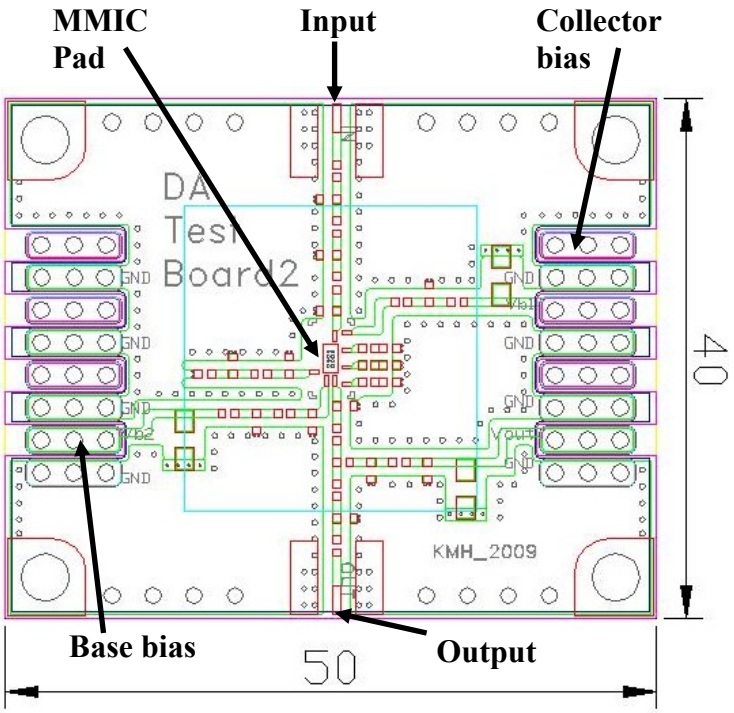

Figure 3.40: Layout of Testboard_2

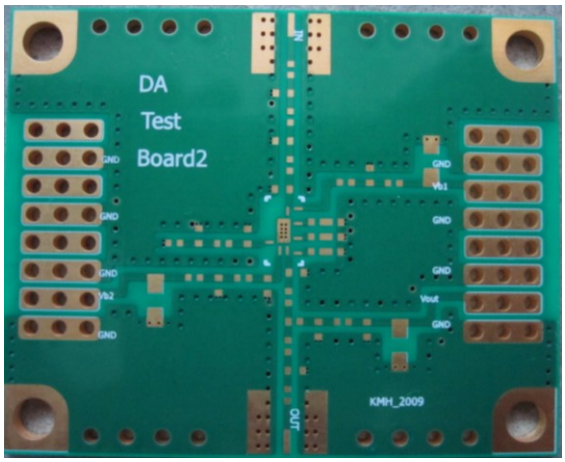

Figure 3.41: Front view of Testboard_2

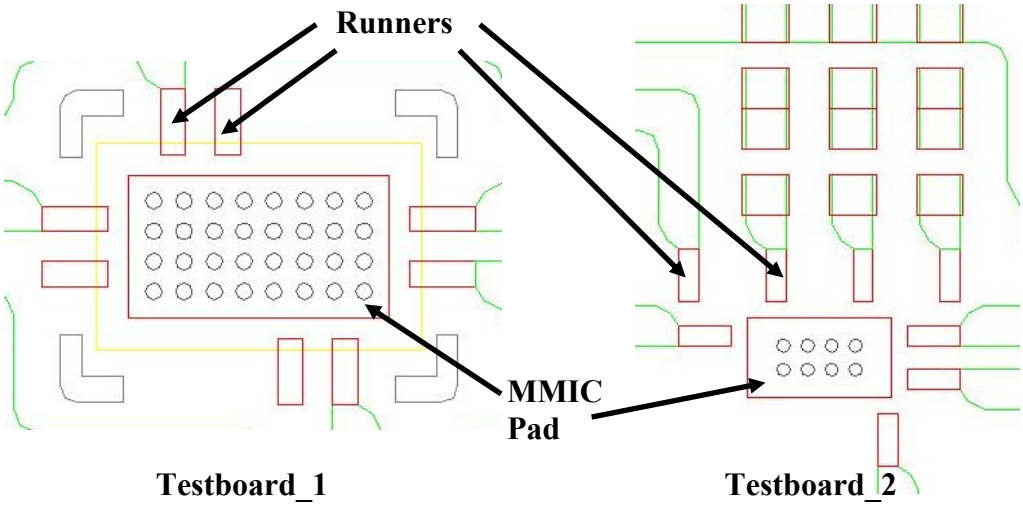

Figure 3.42: Comparison between MMIC pad for Testboard_1 and Testboard_2

3.8 Die Attach

The MMIC DAs were die-attached to the centre of the testboards using the Diemat DM6030Hk-PT/H579 epoxy shown in Fig. 3.43, which has high thermal and electrical conductivity. This conductive epoxy was chosen because the die had backvias that must be grounded to the testboard. The epoxy is applied to the MMIC pad using a very fine toothpick and the dies from the gel pack shown in Fig. 3.44 are then picked using a tweezer and placed onto the testboard.

Once the dies have been placed on top of the epoxy, the testboards will be placed into an oven for the curing process. Fig. 3.45 is the metal cage used to store the boards when they are in the oven. The curing process takes 1 hour and 20 minutes. The temperature will be ramped up to 175 ^{o}C within 30 minutes and maintained at that temperature for another 50 minutes.

Figure 3.43: Diemat conductive epoxy

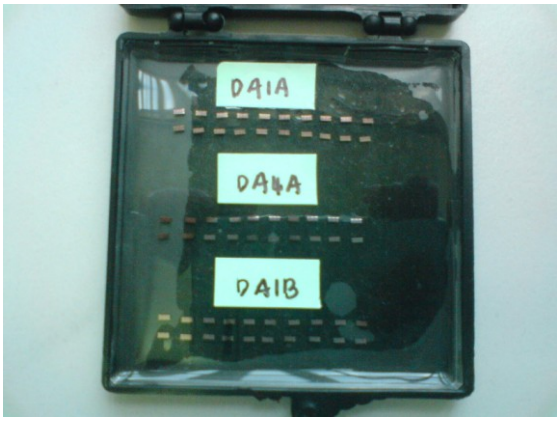

Figure 3.44: MMIC DA in gel pack

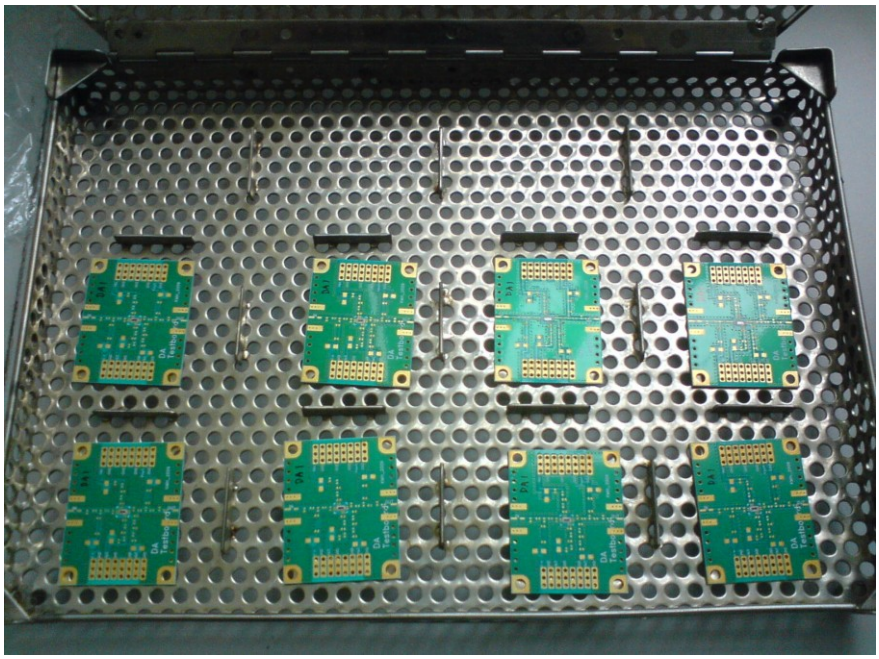

Figure 3.45: Testboards awaiting curing process

3.9 Wire-bonding

Wirebonding is the main method of making connections between an integrated circuit (IC) and the printed circuit board (PCB). The bondwires used consist of gold and have a diameter of 1 mil (~25 μm). The Kulicke and Soffa (K&S) 4524 Manual Wire Bonder shown in Fig. 3.46 and 3.47 is used to perform the wire bonding. There are generally two main classes of wire bonding which are ball bonding and wedge bonding. This model of wire bonder performs ball bonding unto the MMIC using a combination of heat, pressure and ultrasonic energy.

Using the multi-mouse, the bonding head can be moved around to the desired location. The gold wires are stored in the spool cup whereas the workholder holds the testboard in place. Settings for the bond parameters can be made using the control pad and right panel.

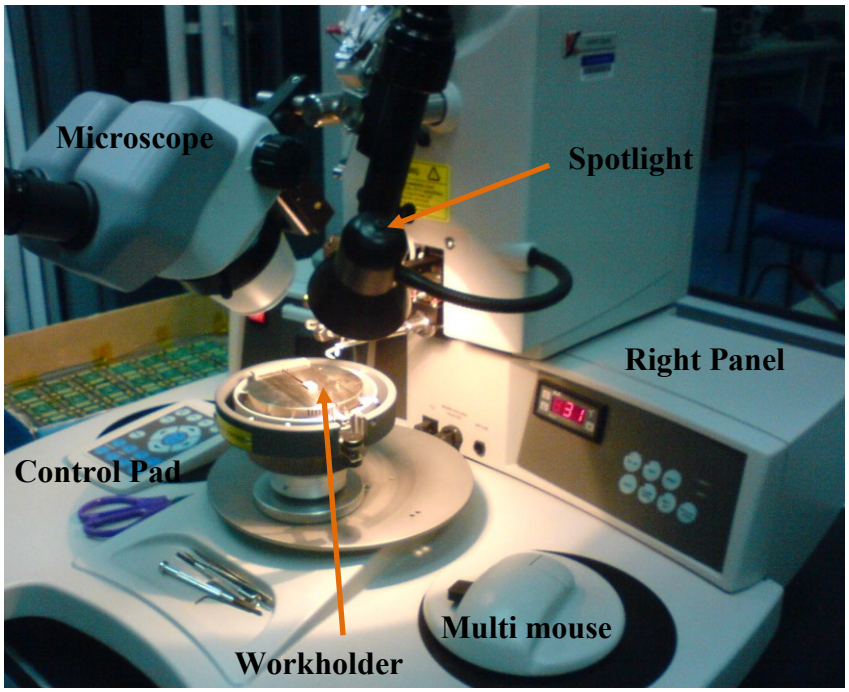

Figure 3.46: Front view of K&S 4524 Manual Wire Bonder

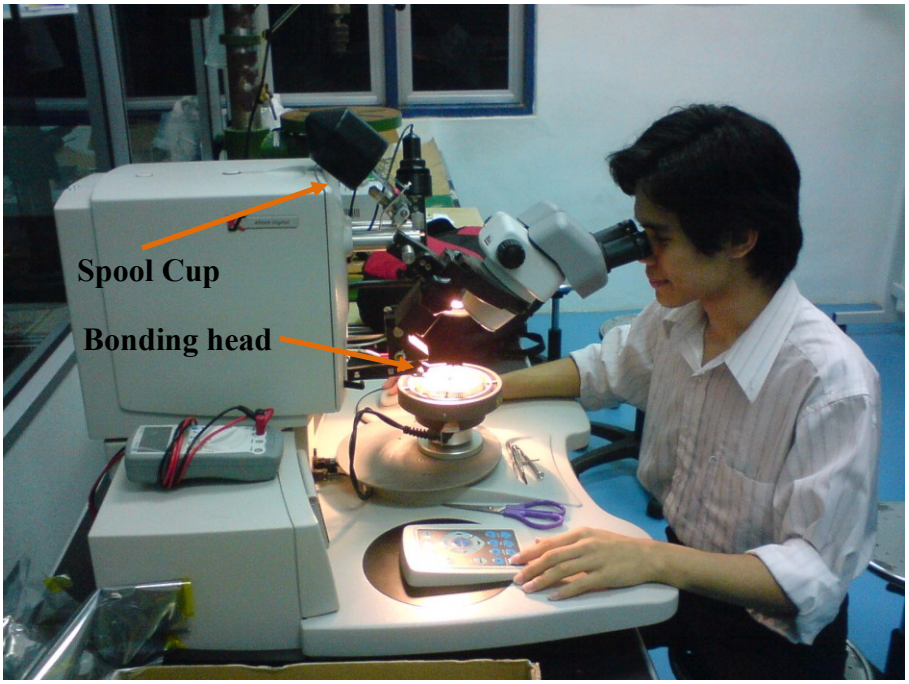

Figure 3.47: Side view of K&S 4524 Manual Wire Bonder

The steps for creating a bond wire are shown in Fig. 3.48.

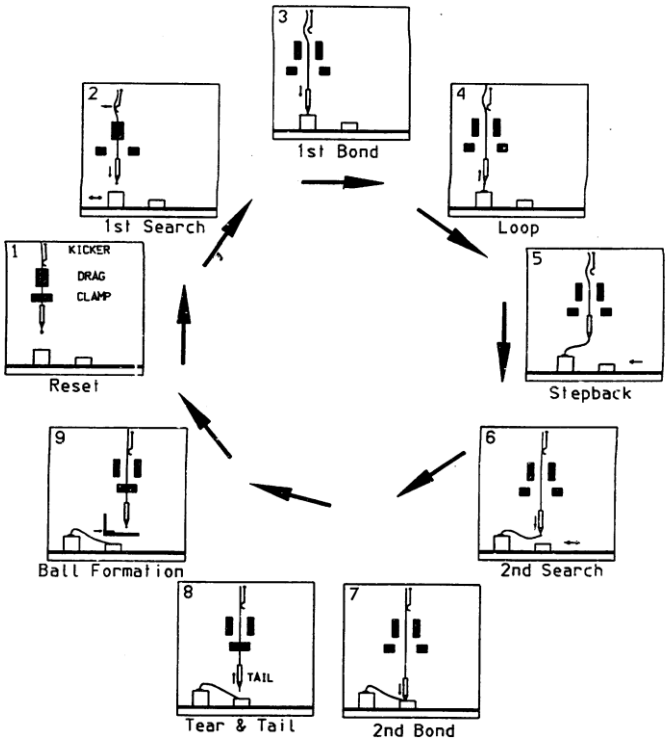

Figure 3.48: Steps for creating a bondwire [120]

Firstly, the capillary searches for the height according to the settings made. Then, a first bond is made to the MMIC. The power, force and time parameters all determine whether there will be a successful bond. For example, if the force is too weak, the ball will not stick but if the force is too strong, it will crack the die. After the first bond is made, the capillary rises to the height determined by the loop parameter. It then steps back and performs a second search for the top layer of the testboard. A second bond is made and this is commonly a stitch bond. The tail parameter determines how much tail the wire should have before the Negative Electric Flame Off (NEFO) sparks and creates a new ball. The size of the new ball is determined by the ball parameter. Table 3.13 shows the bond parameters used in this project.

Table 3.13: Bond parameters

Bond	**Parameter**	**Value**
First Bond	Search	4.46
	Power	2.5
	Time	6.0
	Force	2.0
Second Bond	Search	3.36
	Power	3.21
	Time	6.0
	Force	3.2
	Loop	5.0
	Tail	2.5
	Ball	1.5

Figs. 3.49 and 3.50 show the bond diagrams for DA1 to DA4 and subsequently DA1A, DA1B and DA4A. Fig. 3.51 shows how the actual MMIC is connected to the testboard via bondwires.

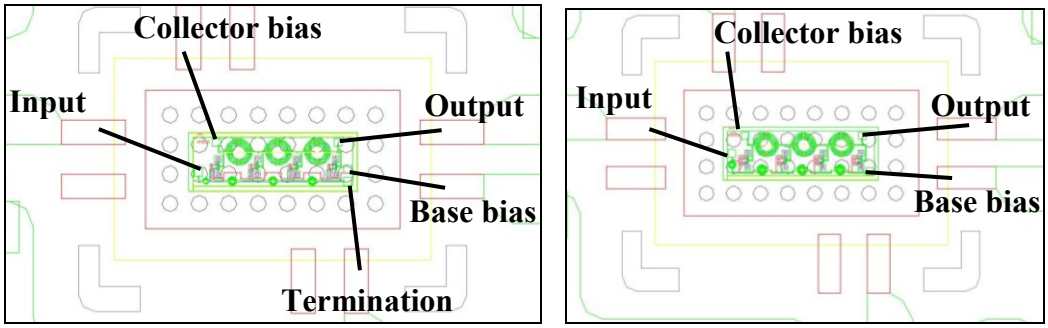

Figure 3.49: (a) Bond diagram for DA1 and DA2 (left)

(b) Bond diagram for DA3 and DA4 (right)

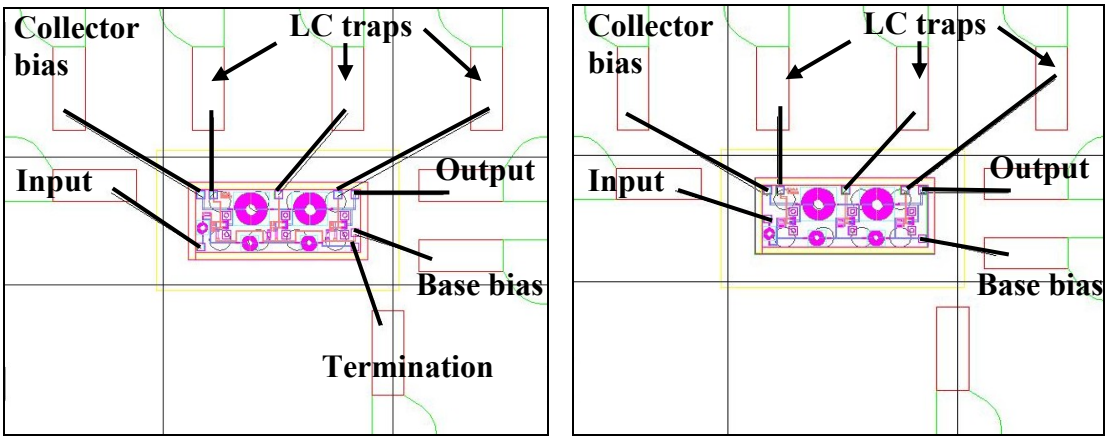

Figure 3.50: (a) Bond diagram for DA1A and DA1B (left)

(b) Bond diagram for DA4A (right)

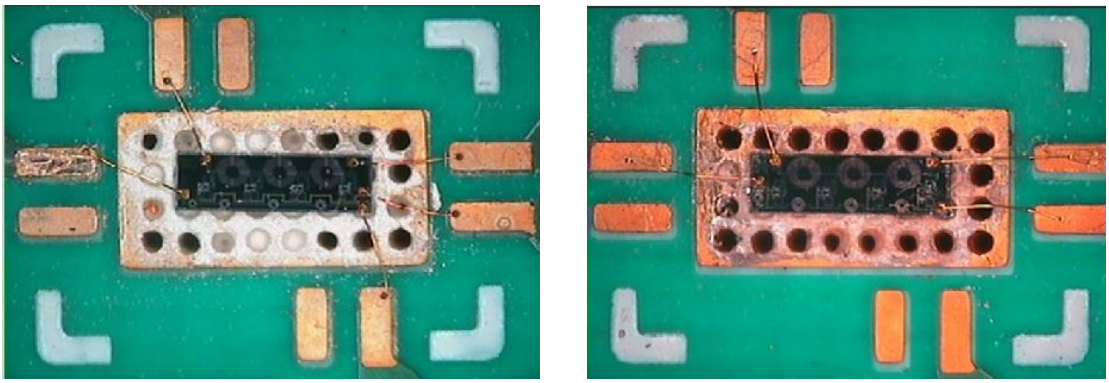

Figure 3.51: (a) Photo of DA1 connected to testboard via bondwires (left)

(b) Photo of DA3 connected to testboard via bondwires (right)

3.10 Testboard Population

Population and soldering of the SMT components onto the testboards were performed at the workstation. Solder paste is fed through a syringe using pneumatic pressure to control the exact amount used. The testboards with the MMIC DA attached to the centre and connected to all the tuning elements and SMA connectors are shown in Figs. 3.52 and 3.53. The values of these components have been shown in Table 3.6 and Table 3.11.

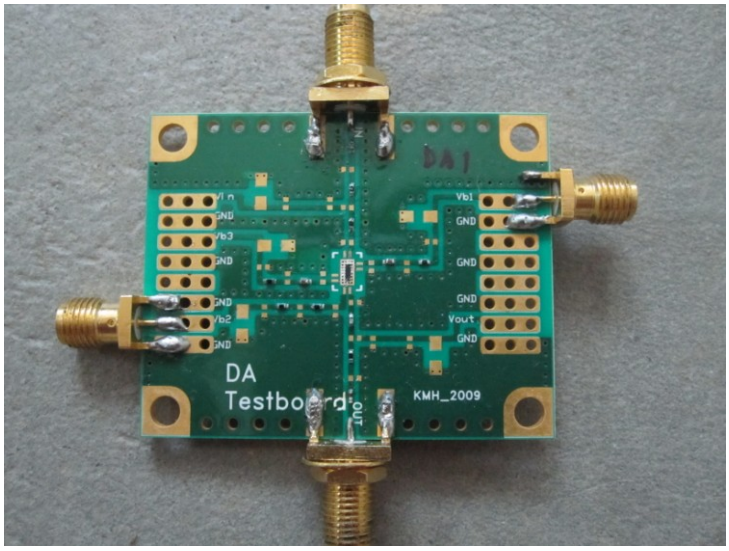

Figure 3.52: Measurement-ready DA (First design)

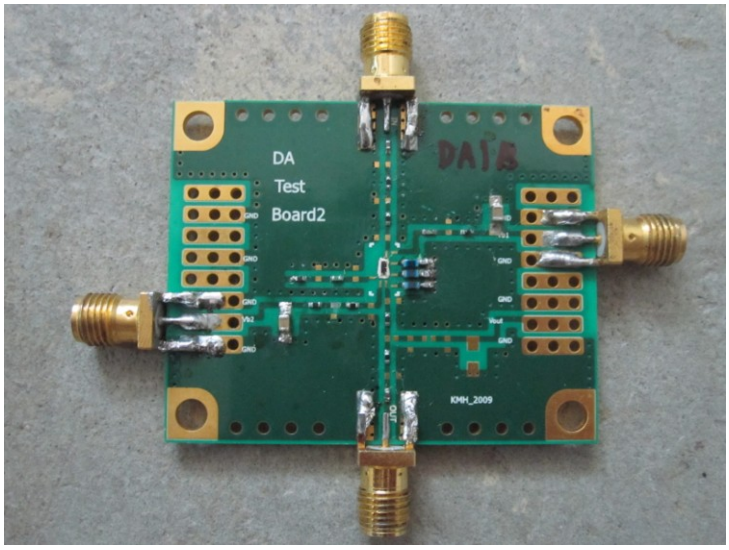

Figure 3.53: Measurement-ready DA (Second design)

3.11 Nonlinearities in HBTs

Despite having highly nonlinear sources, HBTs have the attractive property of high linearity at relatively low levels of DC bias power [121]-[122]. The dependence of the base current, I_b on the base-emitter voltage V_{be} is an exponential function and is a very strong nonlinearity. Furthermore, the base-emitter capacitance which is primarily a diffusion capacitance is also strongly nonlinear.

Before the HBT can be linearized, its nonlinear characteristics must be determined. The nonlinear behaviour of HBTs has been extensively studied [110], [123]-[132] and the main nonlinear sources in the HBT are the base-emitter resistance, r_π, the base-emitter capacitance, C_{be} (which is made up of diffusion and depletion capacitances), the transconductance, g_m and the base-collector capacitance, $C_{bc.}$

C_{bc}, which is a depletion capacitance is the dominant nonlinear source and should be linearized to reduce intermodulation distortions [124]-[129]. A punchthrough collector which linearizes C_{bc}, results in a 3 dB increase in IP3 compared to a conventional collector [125]. Measurements on various emitter, base and collector profiles showed that the collector variations have the most significant influence on intermodulation behavior [127]. InGaP/GaAs HBTs with non-uniform collector doping improves linearity with negligible impact on DC characteristics [129].

From [124], emitter and base resistances linearize the HBT's output and [125] reports that high linearity is a result of the cancellation between the output nonlinear currents generated by the base-emitter and base-collector sources. According to Maas [121], the high linearity in HBTs is due to the partial cancellation between the IM currents generated from the base-emitter (junction) current and the junction capacitance.

The partial cancellation of IM currents from the total base-emitter current and total base-collector current also results in good IP3 [130]. From [110], the nonlinear currents due to r_π and C_{diff}, are canceled almost completely by g_m for all frequencies. The C_{depl} nonlinearity becomes significant at high frequencies. Analytical nonlinear

models for HBTs using Volterra-series analysis have also been developed for nonlinear simulations [131]-[132].

3.11.1 Analysis of Relation Between Low Impedance Termination at Output of HBT to Linearity

Fig. 3.54 shows the HBT circuit with nonlinear elements r_π, C_{be}, g_m and C_{bc}. C_{be} is split into $C_{diffusion}$ and $C_{depletion}$.

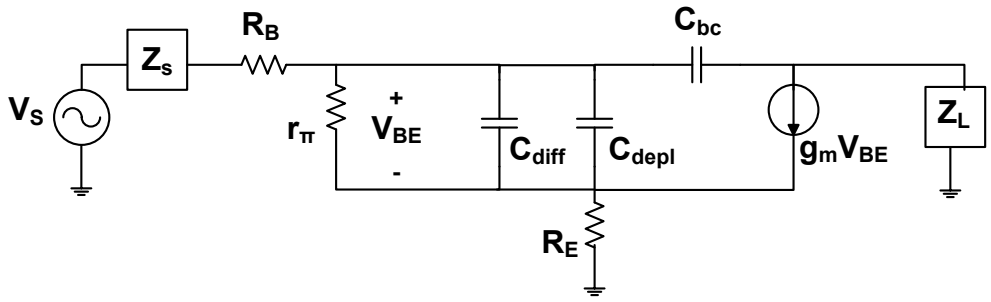

Figure 3.54: HBT circuit model nonlinear elements with C_{bc}

The Gummel–Poon model equation for base-collector capacitance as a function of bias is given by [127]:

$$C_{bc} = C_{jc} X_{cjc} \left(1 - \frac{V_{bc}}{V_{jc}}\right)^{-Mjc} \approx c_0 + c_1 V_{bc} + c_2 V_{bc}^2 \qquad (3.13)$$

where C_{jc} and V_{jc} are the base-collector zero bias capacitance and diffusion voltage respectively. X_{cjc} is the intrinsic fraction of total base-collector capacitance while M_{jc} is the base-collector grading factor. Coefficients c_1 and c_2 are first and second derivatives of C_{bc} with respect to voltage.

Voltage across the base and collector nodes is defined in terms of orders of voltages:

$$V_{bc} = V_{bc1} + V_{bc2} + \ldots \qquad (3.14)$$

where V_{bc1} is the voltage for first order frequencies (such as ω_1 and ω_2) and V_{bc2} is the voltage for second order frequencies (such as ω_2-ω_1 and $2\omega_2$). Current from the base-collector capacitance can be obtained from

$$i_{Cbc} = C_{bc} \frac{\partial V_{bc}}{\partial t} \tag{3.15}$$

From [127], solving for the third order current $i_{Cbc,3}$ (at $2\omega_2$-ω_1) using the method of nonlinear currents:

$$i_{Cbc,3} = c_1 \left(V_{bc2} \frac{\partial V_{bc1}}{\partial t} + V_{bc1} \frac{\partial V_{bc2}}{\partial t} \right) + c_2 V_{bc1}^2 \frac{\partial V_{bc1}}{\partial t} \tag{3.16}$$

It is clear that the third order current depends on the second order base-collector voltage at $2\omega_2$ and ω_2-ω_1. Although placing a trap at the output tunes the V_{ce}, but C_{bc} is a nonlinear capacitance dependent on V_{ce} [124], [128], [133].

3.11.2 Analysis of Relation Between Low Impedance Termination at Input of HBT to Linearity

To analyze the distortion in the HBT, the Volterra series analysis of a simplified HBT circuit is performed using the method of nonlinear currents [74], [121]. The third order intermodulation current, $I_{o,3}$ is primarily dependent on the base-emitter voltage at the envelope frequency, $V_{be,\omega 2-\omega 1}$ and second harmonic, $V_{be,2\omega 2}$. Therefore, by implementing a low impedance termination at the envelope frequency, it is possible to reduce the third order intermodulation current and increase OIP3. It is also possible to increase the OIP3 by tuning the second harmonic.

Wooyun Kim *et. al* [110] takes the analysis performed by Maas further by improving on his equations to account the depletion capacitance in the HBT. The newer model also provides a better definition for the nonlinear collector current in terms of the transconductance and base-emitter voltage.

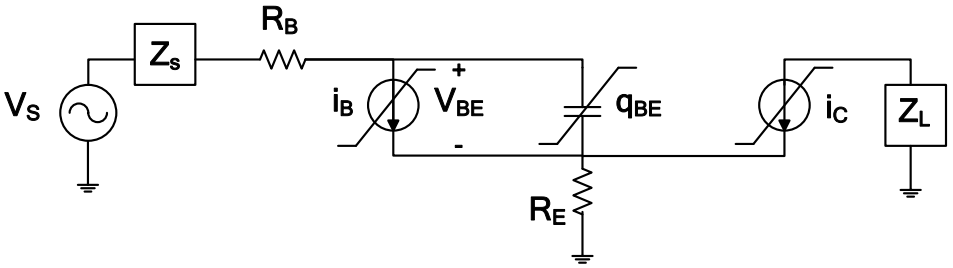

Figure 3.55: HBT nonlinear equivalent circuit model without C_{bc}

The simplified equivalent HBT circuit is shown in Fig. 3.55. The base and collector nonlinear current sources are represented by i_B and i_C, respectively. Base-emitter nonlinear charge appears as q_{BE}. C_{bc} is omitted to simplify the circuit analysis but the model is sufficient to represent most of the nonlinear properties of the HBT.

By third order expansion of the Taylor series, nonlinear elements can be obtained. Under small-signal conditions, the base nonlinear current source can be expanded in the vicinity of its bias point, resulting in

$$i_B = I_{SB}\left(\exp\left(\frac{V_{BE}}{\eta_B V_T}\right)-1\right) \tag{3.17}$$

$$\begin{aligned} i_b &= \frac{I_B}{\eta_B V_T}v_{be} + \frac{I_B}{2\eta_B^2 V_T^2}v_{be}^2 + \frac{I_B}{6\eta_B^3 V_T^3}v_{be}^3 \\ &= g_1 v_{be} + g_2 v_{be}^2 + g_3 v_{be}^3 \end{aligned} \tag{3.18}$$

where I_{SB} is the base saturation current, η_B is the base ideality factor, I_B is the DC base current and V_T is the thermal voltage (≈26 mV). i_b and v_{be} are small signal components for i_B and V_{BE} respectively. The coefficient g_1 is the linearized junction conductance and = $1/r_\pi$.

Using the same analysis performed at the base, the nonlinear current at the collector is given by

$$i_C = I_{SC}\left(\exp\left(\frac{V_{BE}}{\eta_C V_T}\right)-1\right) \tag{3.19}$$

$$
\begin{aligned}
i_c &= \frac{I_C}{\eta_C V_T} v_{be} + \frac{I_C}{2\eta_C^2 V_T^2} v_{be}^2 + \frac{I_C}{6\eta_C^3 V_T^3} v_{be}^3 \\
&= g_{m1} v_{be} + g_{m2} v_{be}^2 + g_{m3} v_{be}^3
\end{aligned}
\tag{3.20}
$$

where I_{SC} is the collector saturation current, η_C is the collector ideality factor, I_C is the DC collector current. i_c is the small signal components for I_C whereas g_{m1} is the transconductance of the device.

The stored charge at the base-emitter junction, q_{BE} is the sum of diffusion and depletion charges. It can be expanded to

$$
\begin{aligned}
q_{be} &= \left(C_{diff} + C_{depl}\right) v_{be} \\
&\quad + \left(\frac{I_C}{2\eta_C^2 V_T^2} \tau_B + \frac{I_B}{2\eta_B^2 V_T^2} \tau_E + \frac{C_{depl}}{4\left(V_{bi} - V_{BE}\right)} \right) v_{be}^2 \\
&\quad + \left(\frac{I_C}{6\eta_C^3 V_T^3} \tau_B + \frac{I_B}{6\eta_B^3 V_T^3} \tau_E + \frac{C_{depl}}{8\left(V_{bi} - V_{BE}\right)^2} \right) v_{be}^3 \\
&= c_1 v_{be} + c_2 v_{be}^2 + c_3 v_{be}^3
\end{aligned}
\tag{3.21}
$$

where

$$
C_{diff} = \frac{I_C}{\eta_C V_T} \tau_B + \frac{I_B}{\eta_B V_T} \tau_E \tag{3.22}
$$

and

$$
C_{depl} = A_E \sqrt{\frac{q \varepsilon_E \varepsilon_B N_E P_B}{2\left(\varepsilon_E N_E + \varepsilon_B P_B\right)\left(V_{bi} - V_{BE}\right)}} \tag{3.23}
$$

V_{bi} is the built-in potential of the base-emitter junction and V_{BE} is the base-emitter DC bias voltage. q_{be} is the small-signal component of q_{BE}. c_1 is the base-emitter capacitance C_π.

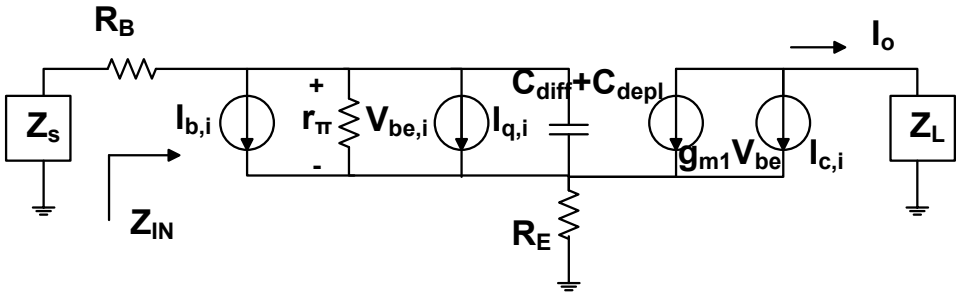

Figure 3.56: HBT equivalent circuit for second and third order intermodulation analysis

The equivalent circuit model used for the second order analysis is shown in Fig. 3.56. The impedance Z_{IN} and Z_π is given by

$$Z_{IN} = \left(R_B + Z_\pi + R_E\left(1 + Z_\pi g_m\right)\right) \tag{3.24}$$

$$Z_\pi = \left(r_\pi \parallel C_{diff} \parallel C_{depl}\right) \tag{3.25}$$

At frequency $2\omega_2$, $1/Z_\pi$ becomes

$$\frac{1}{Z_{\pi,2\varpi_2}} = \left(g_1 + j2\omega_2 c_1\right) \tag{3.26}$$

The second order nonlinear currents generated by the base-emitter junction capacitance, $I_{q,2}$ and the nonlinear base and collector currents, $I_{b,2}$ and $I_{c,2}$ are

$$I_{q,2} = \frac{1}{4} c_2 \sum_{i=-2}^{2}\sum_{k=-2}^{2} V_{be,\omega_i} V_{be,\omega_k}\, j\left(\omega_i + \omega_k\right).\exp\left(j\left(\omega_i + \omega_k\right)t\right) \tag{3.27}$$

$$I_{b,2} = \frac{1}{4} g_2 \sum_{i=-2}^{2}\sum_{k=-2}^{2} V_{be,\omega_i} V_{be,\omega_k}.\exp\left(j\left(\omega_i + \omega_k\right)t\right) \tag{3.28}$$

$$I_{c,2} = \frac{1}{4} g_{m2} \sum_{i=-2}^{2}\sum_{k=-2}^{2} V_{be,\omega_i} V_{be,\omega_k}\, j\left(\omega_i + \omega_k\right).\exp\left(j\left(\omega_i + \omega_k\right)t\right) \tag{3.29}$$

where $V_{be,\omega i}$ is the first order voltage phasor of V_{be} at the excitation frequency ω_i.

Thus, the second order IM current source for frequency $2\omega_2$ is

$$I_{q,2\omega_2} = \frac{1}{2} j(2\omega_2) c_2 V_{be,\omega_2}^2 \tag{3.30}$$

$$I_{b,2\omega_2} = \frac{1}{2} g_2 V_{be,\omega_2}^2 \tag{3.31}$$

$$I_{c,2\omega_2} = \frac{1}{2} g_{m2} V_{be,\omega_2}^2 \tag{3.32}$$

Performing a linear analysis on the circuit, the base-to-emitter junction voltage at the second harmonic is

$$\begin{aligned} V_{be,2\omega_2} &= \frac{Z_\pi}{Z_{IN} + Z_S} V_{S,2\omega_2} \\ &= \frac{-\left(Z_{S,2\omega_2} + R_B + R_E\right) Z_{\pi,2\omega_2} \left(I_{b,2\omega_2} + I_{q,2\omega_2}\right) - R_E Z_{\pi,2\omega_2} I_{c,2\omega_2}}{Z_{IN,2\omega_2} + Z_{S,2\omega_2}} \end{aligned} \tag{3.33}$$

The output current, $I_{o,2\omega 2}$ at the second harmonic frequency is

$$I_{o,2\omega_2} = g_{m1} V_{be,2\omega_2} + I_{c,2\omega_2} \tag{3.34}$$

Substituting (3.33) into (3.34) results in

$$\begin{aligned} I_{o,2\omega_2} &= \frac{-g_{m1}\left(Z_{S,2\omega_2} + R_B + R_E\right) Z_{\pi,2\omega_2}}{Z_{IN,2\omega_2} + Z_{S,2\omega_2}} I_{b,2\omega_2} \\ &+ \frac{-g_{m1}\left(Z_{S,2\omega_2} + R_B + R_E\right) Z_{\pi,2\omega_2}}{Z_{IN,2\omega_2} + Z_{S,2\omega_2}} I_{q,2\omega_2} \\ &- \frac{R_E Z_{\pi,2\omega_2}}{Z_{IN,2\omega_2} + Z_{S,2\omega_2}} I_{c,2\omega_2} + \frac{Z_{IN,2\omega_2} + Z_{S,2\omega_2}}{Z_{IN,2\omega_2} + Z_{S,2\omega_2}} I_{c,2\omega_2} \end{aligned} \tag{3.35}$$

Substituting $Z_{IN,2\omega 2}$ in (3.24) into the fourth term of (3.35) results in

$$\begin{aligned} I_{o,2\omega_2} &= \frac{-g_{m1}\left(Z_{S,2\omega_2}+R_B+R_E\right)Z_{\pi,2\omega_2}}{Z_{IN,2\omega_2}+Z_{S,2\omega_2}}\left(I_{b,2\omega_2}+I_{q,2\omega_2}\right) \\ &+\frac{\left(Z_{\pi,2\omega_2}+Z_{S,2\omega_2}+R_B+R_E\right)Z_{\pi,2\omega_2}}{Z_{IN,2\omega_2}+Z_{S,2\omega_2}}I_{c,2\omega_2} \end{aligned} \tag{3.36}$$

Since the circuit in Fig. 3.56 also applies to third order intermodulation, the third order currents at frequency $2\omega_2$-ω_1 are

$$\begin{aligned} I_{q,2\omega_2-\omega_1} &= j(2\omega_2-\omega_1)\frac{3}{4}c_3V_{be,\omega_2}^2V_{be,\omega_1}^* + j(2\omega_2-\omega_1)c_2\left[V_{be,2\omega_2}V_{be,\omega_1}^* + V_{be,\omega_2}V_{be,\omega_2-\omega_1}\right] \\ &= j(2\omega_2-\omega_1)\left[\frac{3}{4}c_3+c_2X\right]V_{be,\omega_2}^2V_{be,\omega_1}^* \end{aligned} \tag{3.37}$$

$$\begin{aligned} I_{b,2\omega_2-\omega_1} &= \frac{3}{4}g_3V_{be,\omega_2}^2V_{be,\omega_1}^* + g_2\left[V_{be,2\omega_2}V_{be,\omega_1}^* + V_{be,\omega_2}V_{be,\omega_2-\omega_1}\right] \\ &= \left[\frac{3}{4}g_3+g_2X\right]V_{be,\omega_2}^2V_{be,\omega_1}^* \end{aligned} \tag{3.38}$$

$$\begin{aligned} I_{c,2\omega_2-\omega_1} &= \frac{3}{4}g_{m3}V_{be,\omega_2}^2V_{be,\omega_1}^* + g_{m2}\left[V_{be,2\omega_2}V_{be,\omega_1}^* + V_{be,\omega_2}V_{be,\omega_2-\omega_1}\right] \\ &= \left[\frac{3}{4}c_3+c_2X\right]V_{be,\omega_2}^2V_{be,\omega_1}^* \end{aligned} \tag{3.39}$$

where coefficient X is defined as follows

$$\begin{aligned} X &= \frac{V_{be,2\omega_2}V_{be,\omega_1}^*}{V_{be,\omega_2}^2V_{be,\omega_1}^*} + \frac{V_{be,\omega_2}V_{be,\omega_2-\omega_1}}{V_{be,\omega_2}^2V_{be,\omega_1}^*} \\ &= \frac{V_{be,2\omega_2}}{V_{be,\omega_2}^2} + \frac{V_{be,\omega_2-\omega_1}}{V_{be,\omega_2}V_{be,\omega_1}^*} \end{aligned} \tag{3.40}$$

Substituting (3.33) and its equivalent for $V_{be,\omega 1-\omega 2}$ into (3.40) gives

$$X = -\left[\begin{array}{l} \dfrac{\left(Z_{S,2\omega_2}+R_B+R_E\right)Z_{\pi,2\omega_2}\left(I_{b,2\omega_2}+I_{q,2\omega_2}\right)+R_E Z_{\pi,2\omega_2} I_{c,2\omega_2}}{\dfrac{Z_{IN,2\omega_2}+Z_{S,2\omega_2}}{V_{be,\omega_2}^2}} \\ +\dfrac{\left(Z_{S,\omega_2-\omega_1}+R_B+R_E\right)Z_{\pi,\omega_2-\omega_1}\left(I_{b,\omega_2-\omega_1}+I_{q,\omega_2-\omega_1}\right)+R_E Z_{\pi,\omega_2-\omega_1} I_{c,\omega_2-\omega_1}}{\dfrac{Z_{IN,\omega_2-\omega_1}+Z_{S,\omega_2-\omega_1}}{V_{be,\omega_2}V_{be,\omega_1}^*}} \end{array}\right] \tag{3.41}$$

Substituting (3.30) – (3.32) and its equivalent for nonlinear currents at ω_2-ω_1 into (3.41) results in

$$X = -\left[\begin{array}{l} \dfrac{\left(Z_{S,2\omega_2}+R_B+R_E\right)Z_{\pi,2\omega_2}\left(\dfrac{1}{2}g_2 V_{be,\omega_2}^2+\dfrac{1}{2}j\omega_2 2c_2 V_{be,\omega_2}^2\right)}{\dfrac{Z_{IN,2\omega_2}+Z_{S,2\omega_2}}{V_{be,\omega_2}^2}} \\ +\dfrac{R_E Z_{\pi,2\omega_2}\dfrac{1}{2}g_{m2}V_{be,\omega_2}^2}{\dfrac{Z_{IN,2\omega_2}+Z_{S,2\omega_2}}{V_{be,\omega_2}^2}} \\ +\dfrac{\left(Z_{S,\omega_2-\omega_1}+R_B+R_E\right)Z_{\pi,\omega_2-\omega_1}\left(g_2 V_{be,\omega_2}V_{be,\omega_1}^*+j(\omega_2-\omega_1)c_2 V_{be,\omega_2}V_{be,\omega_1}^*\right)}{\dfrac{Z_{IN,\omega_2-\omega_1}+Z_{S,\omega_2-\omega_1}}{V_{be,\omega_2}V_{be,\omega_1}^*}} \\ +\dfrac{R_E Z_{\pi,\omega_2-\omega_1} g_{m2} V_{be,\omega_2}V_{be,\omega_1}^*}{\dfrac{Z_{IN,\omega_2-\omega_1}+Z_{S,\omega_2-\omega_1}}{V_{be,\omega_2}V_{be,\omega_1}^*}} \end{array}\right] \tag{3.42}$$

Substituting (3.36) and its equivalent into (3.42) gives

$$X = -\left[\begin{array}{l} \dfrac{\left(Z_{S,2\omega_2} + R_B + R_E\right)Z_{\pi,2\omega_2}\left(\dfrac{1}{2}g_2 + \dfrac{1}{2}j\omega_2 2c_2\right) + R_E Z_{\pi,2\omega_2}\dfrac{1}{2}g_{m2}}{\left(R_B + Z_{\pi,2\omega_2} + R_E + R_E Z_{\pi,2\omega_2} g_{m1}\right) + Z_{S,2\omega_2}} \\ + \dfrac{\left(Z_{S,\omega_2-\omega_1} + R_B + R_E\right)Z_{\pi,\omega_2-\omega_1}\left(g_2 + j(\omega_2-\omega_1)c_2\right) + R_E Z_{\pi,\omega_2-\omega_1} g_{m2}}{\left(R_B + Z_{\pi} + R_E + R_E Z_{\pi,\omega_2-\omega_1} g_{m1}\right) + Z_{S,\omega_2-\omega_1}} \end{array}\right]$$

$$= -\left[\begin{array}{l} \dfrac{\left(Z_{S,2\omega_2} + R_B + R_E\right)\left(\dfrac{1}{2}g_2 + \dfrac{1}{2}j\omega_2 2c_2\right) + R_E\dfrac{1}{2}g_{m2}}{1 + R_E g_{m1} + \left(\dfrac{Z_{S,2\omega_2} + R_B + R_E}{Z_{\pi,2\omega_2}}\right)} \\ + \dfrac{\left(Z_{S,\omega_2-\omega_1} + R_B + R_E\right)\left(g_2 + j(\omega_2-\omega_1)c_2\right) + R_E g_{m2}}{1 + R_E g_{m1} + \left(\dfrac{Z_{S,\omega_2-\omega_1} + R_B + R_E}{Z_{\pi,\omega_2-\omega_1}}\right)} \end{array}\right]$$

$$= -\left[\begin{array}{l} \dfrac{\left(Z_{S,2\omega_2} + R_B + R_E\right)\left(g_2 + j2\omega_2 c_2\right) + R_E g_{m2}}{2\left(1 + \left(Z_{S,2\omega_2} + R_B + R_E\right)\left(g_1 + j2\omega_2 c_1\right) + R_E g_{m1}\right)} \\ + \dfrac{\left(Z_{S,\omega_1-\omega_2} + R_B + R_E\right)\left(g_2 + j(\omega_2-\omega_1)c_2\right) + R_E g_{m2}}{1 + \left(Z_{S,\omega_2-\omega_1} + R_B + R_E\right)\left(g_1 + j(\omega_2-\omega_1)c_1\right) + R_E g_{m1}} \end{array}\right] \tag{3.43}$$

The third order V_{be} is given as

$$V_{be,2\omega_2-\omega_1} = \frac{R_E Z_{\pi,2\omega_2-\omega_1}(I_{b,2\omega_2-\omega_1} + I_{q,2\omega_2-\omega_1}) - R_E Z_{\pi,2\omega_2-\omega_1} I_{c,2\omega_2-\omega_1}}{Z_{IN,2\omega_2-\omega_1} + Z_{S,2\omega_2-\omega_1}} \tag{3.44}$$

The total third order intermodulation output current at the collector becomes

$$I_{o,2\omega_2-\omega_1} = g_{m1} V_{be,2\omega_2-\omega_1} + I_{c,2\omega_2-\omega_1} \tag{3.45}$$

Substituting (3.37) – (3.39) and (3.44) into (3.45) results in

$$
\begin{aligned}
I_{o,2\omega_2-\omega_1} &= \frac{-g_{m1}\left(Z_{S,2\omega_2-\omega_1}+R_B+R_E\right)Z_{\pi,2\omega_2-\omega_1}I_{b,2\omega_2-\omega_1}+I_{q,2\omega_2-\omega_1}}{Z_{IN,2\omega_2-\omega_1}+Z_{S,2\omega_2-\omega_1}} \\
&- \frac{-g_{m1}R_E Z_{\pi,2\omega_2-\omega_1}I_{c,2\omega_2-\omega_1}}{Z_{IN,2\omega_2-\omega_1}+Z_{S,2\omega_2-\omega_1}} \\
&+ \frac{\left[Z_{\pi,2\omega_2-\omega_1}+\left(Z_{S,2\omega_2-\omega_1}+R_B+R_E\right)+R_E g_{m1}Z_{\pi,2\omega_2-\omega_1}\right]I_{c,2\omega_2-\omega_1}}{Z_{IN,2\omega_2-\omega_1}+Z_{S,2\omega_2-\omega_1}} \\
&= \frac{\left(Z_{S,2\omega_2-\omega_1}+R_B+R_E\right)Z_{\pi,2\omega_2-\omega_1}}{Z_{IN,2\omega_2-\omega_1}+Z_{S,2\omega_2-\omega_1}} \\
&\bullet \begin{bmatrix} \frac{3}{4}\left(g_1 g_{m3}-g_3 g_{m1}\right)+X\left(g_1 g_{m2}-g_2 g_{m1}\right) \\ +\frac{3}{4}j\left(2\omega_2-\omega_1\right)\left(c_1 g_{m3}-c_3 g_{m1}\right) \\ +j\left(2\omega_2-\omega_1\right)X\left(c_1 g_{m2}-c_2 g_{m1}\right) \end{bmatrix} V_{be,\omega_2}^2 V_{be,\omega_1}^* \\
&+ \frac{Z_{\pi,2\omega_2-\omega_1}}{Z_{IN,2\omega_2-\omega_1}+Z_{S,2\omega_2-\omega_1}}\left(\frac{3}{4}g_{m3}+Xg_{m2}\right)V_{be,\omega_2}^2 V_{be,\omega_1}^*
\end{aligned}
\tag{3.46}
$$

The dependency of $I_{o,2\omega2-\omega1}$ on the base-emitter voltage at the envelope frequency, $V_{be,\omega2-\omega1}$ stems from the fact that the third order nonlinear currents $I_{q,2\omega2-\omega1}$, $I_{b,2\omega2-\omega1}$ and $I_{c,2\omega2-\omega1}$ that make up $I_{o,2\omega2-\omega1}$ are dependent on $V_{be,\omega2-\omega1}$ (from equation (3.37) to (3.39)).

The coefficient X defined in (3.43) and used in (3.46) show that the $V_{be,\omega2-\omega1}$ terms affect the third order IM current. This $V_{be,\omega2-\omega1}$ term can be reduced by simply controlling $Z_{S,\omega2-\omega1}$ as can be seen in Fig. 3.56. It is clear that third order IM currents are dependent on the second harmonic, $Z_{S,2\omega2}$ as well. However, tuning for the second harmonic is not feasible for a broadband application and will be disregarded since it will affect the in-band response of the DA.

To illustrate how the source impedance at the envelope frequency can increase the OIP3 and to obtain the optimum values for the LC trap, the third order power for intermodulation current, $|I_{o,2\omega_2-\omega_1}|^2$ of a single HBT transistor using the

WIN H02U-43 process, is calculated using MATLAB R2006A based on (3.46) using different source impedances at the envelope frequency (10 MHz), $Z_{S,\omega 1-\omega 2}$. First, the resistance is kept constant and the reactance is varied. Then, a 3-D plot of third order power with varying resistance and reactance for the trap is shown. Values of coefficients in (3.43) and (3.46) are calculated based on the transistor data given in [119] and are shown in Table 3.14. The MATLAB codes for the simulation are shown in Appendix A.

Table 3.14: Coefficients for third order intermodulation current analysis

Parameter	Description	Value
g_{m1}	First order transconductance	1.0894 S
g_{m2}	Second order transconductance	20.9505 S
g_{m3}	Third order transconductance	268.5956 S
g_1	First order junction conductance	0.0158 S
g_2	Second order junction conductance	0.3038 S
g_3	Third order junction conductance	3.8953 S
c_1	First order junction capacitance	3.5145 pF
c_2	Second order junction capacitance	62.885 pF
c_3	Third order junction capacitance	805.80 pF
R_B	Base degeneration resistor	4.65 Ω
R_E	Emitter degeneration resistor	1.05 Ω
T_f	Ideal forward transit time	3 ps

The first to third order conductance is obtained using (3.18) while the transconductance is calculated based on (3.20). The junction capacitance is a sum of the base-emitter diffusion and depletion capacitances and calculated from (3.21). $C_{diffusion}$ is defined as T_f * g_m whereas $C_{depletion}$ can be derived from (3.11). It is assumed that $\eta \approx 1$ for the above calculations.

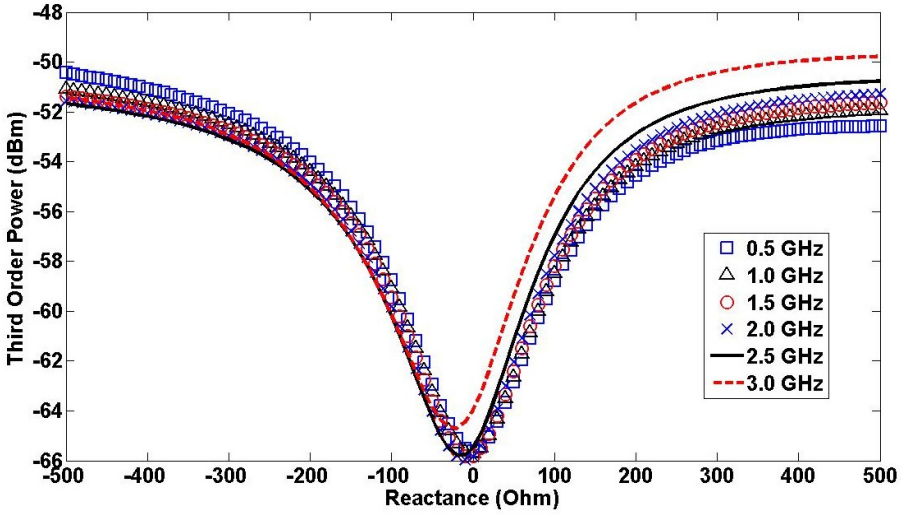

Figure 3.57: Third order power (for intermodulation current) versus reactance values for LC trap

The result of the simulation is shown in Fig. 3.57, where it can be seen that the optimum impedance for the LC trap is a small capacitive reactance at the envelope frequency. Furthermore, based on the simulation results above and (2.12), there is a maximum reduction of 15 dB in third order power resulting in a 7.5 dB increase in OIP3. Equation (2.12) states that the OIP3 is equal to the power at the fundamental tone added with half of the difference between the power for the fundamental tone and third order tone.

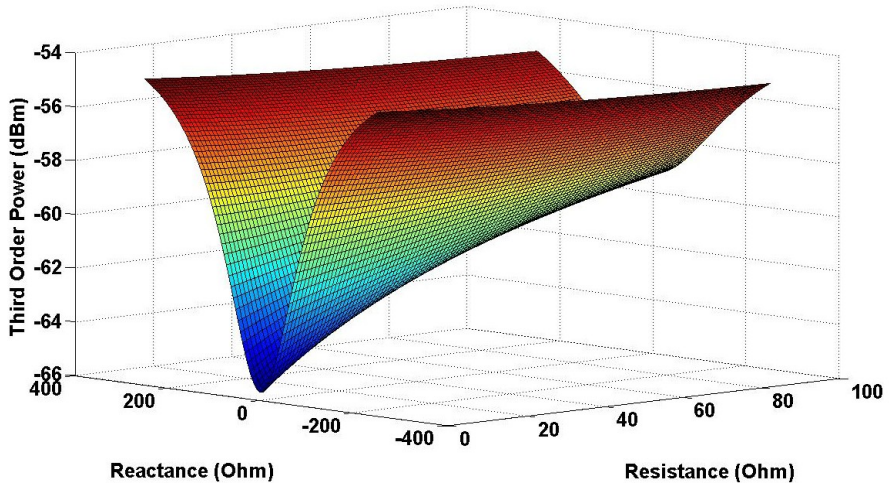

Figure 3.58: Third order power (for intermodulation current) versus resistance and reactance for LC trap at 1 GHz

By maintaining the frequency (1 GHz in the case shown above), the resistance and reactance of the LC trap are varied. As shown in Fig. 3.58, a nearly short circuit (resistance = 0 Ohm) with a small capacitive reactance results in the lowest third order power.

Although C_{bc} is usually the dominant nonlinear source, it is isolated and can be altered by placing the low impedance termination (LC trap) at the input (base) as well as the output (collector) of the HBT, the other nonlinear sources r_{π}, g_m and C_{be} are mainly dependent on the impedance at the envelope frequency presented to the input of the HBT. From the formulae, putting the termination at the input directly affects the r_{π}, g_m and C_{be} nonlinearities and can result in much higher improvement in OIP3 compared to placing it on the output. This is shown by both measured and simulated results shown in Section 4.2.3.1 and Section 4.3.3.2.

3.12 Simulation Setup

Simulations of the S-parameters, P_{1dB} and OIP3 were carried out in ADS using the HBT design kit supplied by WIN Semiconductors. The design kit includes the large signal Vertical Bipolar Intercompany (VBIC) model for the RQ1A202F2_M2 transistor as well as models for the passive components used in the MMIC DA design (spiral inductors, MIM capacitors and thin film resistors). P_{1dB} and OIP3 are simulations that require a large signal model for accuracy.

The Vertical Bipolar Inter Company (VBIC) model was first published in 1995 [21] as an extension of the Kull *et. al* model and developed as a replacement for the SPICE Gummel-Poon (SGP) model. It is important to note that Gummel-Poon and VBIC models were originally developed for silicon based devices. The advantages of VBIC over the Gummel-Poon model are:

i. Base current defined independently without a fixed current parameter
ii. Parasitic substrate transistor
iii. Improved Kull model for quasi saturation
iv. Webster effect

v. Early effect improved compared to SGP
vi. Excess transit time due to base pushout
vii. Partitioning base-emitter junction to intrinsic and extrinsic parts
viii. Partitioning base-emitter capacitance to intrinsic and extrinsic parts
ix. BE and BC breakdown
x. Self-heating
xi. Improved temperature modelling

Ideal lumped components cannot be used in the simulations of the external tuning elements since they do not include effects of parasitics such as series resonance frequency (SRF) and do not accurately model the behaviour of the components especially at high frequencies. Therefore, the design kit from Murata [134] is obtained which includes the S-parameter files for the tuning components used for the DA. However, for the LC trap components, the inductor and capacitor components are rather large and have a low SRF. Murata did not extract the values for frequencies past SRF and so the ADS simulator will extrapolate the data for the component. For example, the Murata data for a 100 nH inductor is only up to 3.3 GHz.

Thus, for the LC trap, Modelithics™ models [135] are used. Accurate S-parameters for the components up to 6 GHz are needed since this is the second harmonic frequency for the upper limit of our amplifier (3 GHz). Equation (3.46) states that the second harmonic impedance, $Z_{2\omega 2}$ plays a role in determining the third order current.

In the following sections, the term “baseline” is the measurement done without the inductor-capacitor network (LC trap) added to the circuit. If traps are placed, the term “with LC trap” is used.

3.12.1 Murata and Modelithics™ SMT Components

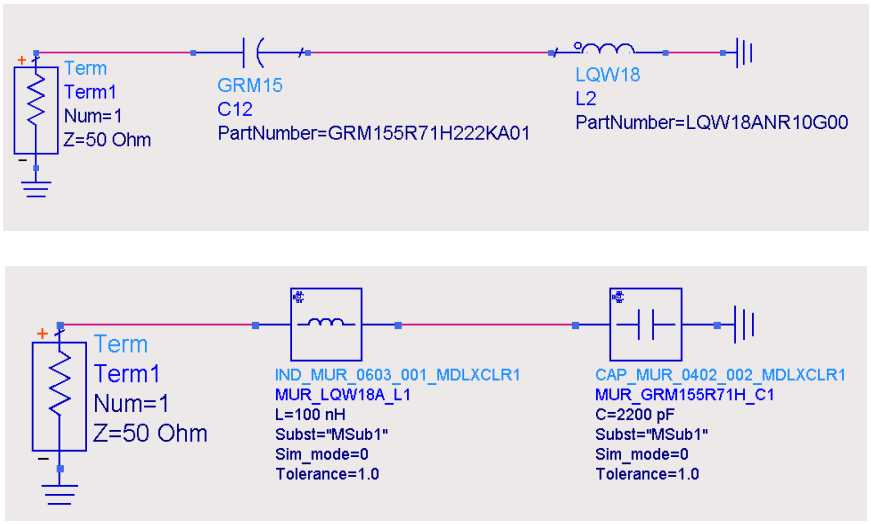

Figure 3.59: (a) ADS models of Murata components for LC trap (top)

(b) ADS models of Modelithics™ components for LC trap (bottom)

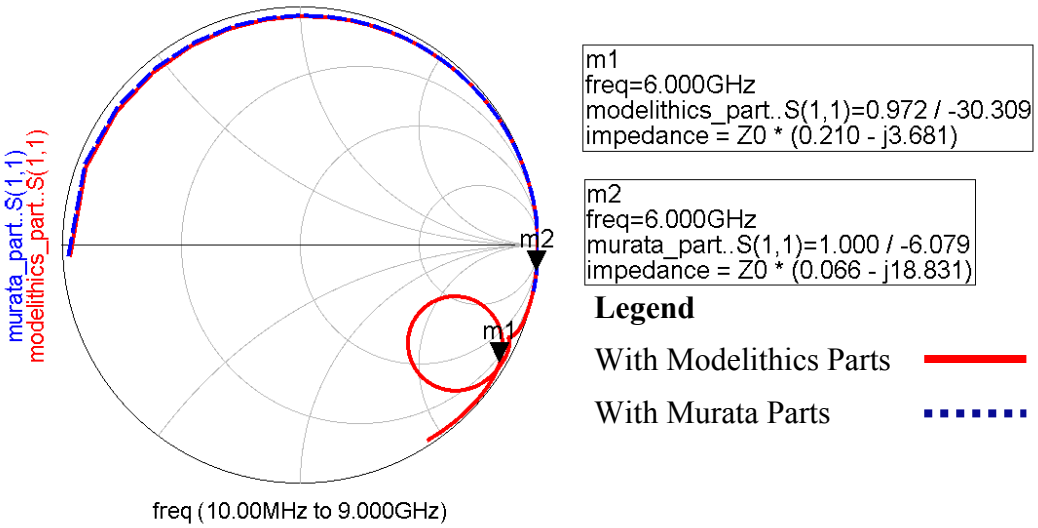

Figure 3.60: Simulation results up to 6 GHz for Murata and Modelithics™ parts

Fig. 3.59 displays the Murata and Modelithics™ 100 nH and 2.2 nF components for the LC trap used in ADS. Fig. 3.60 is the S_{11} results comparing the two. It can be seen that at high frequencies, the Modelithics™ model shows the actual behaviour of the components. The Murata data is extrapolated after 3.3 GHz.

3.12.2 Electromagnetic Simulation of Testboards in Sonnet™

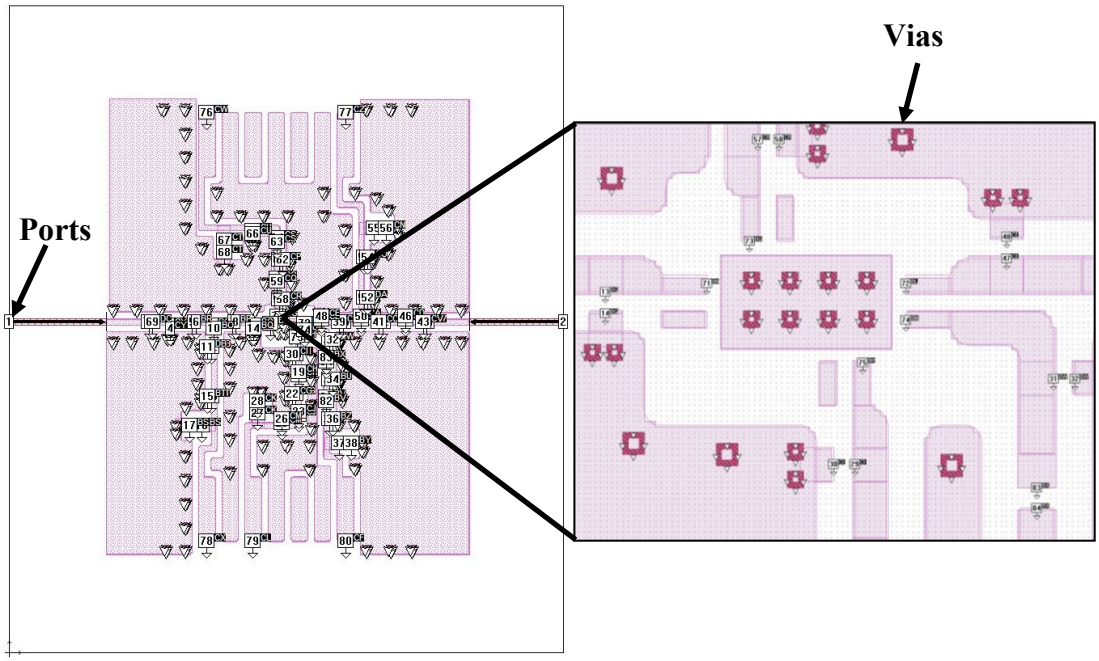

Figure 3.61: Sonnet.geo simulation model of Testboard_1

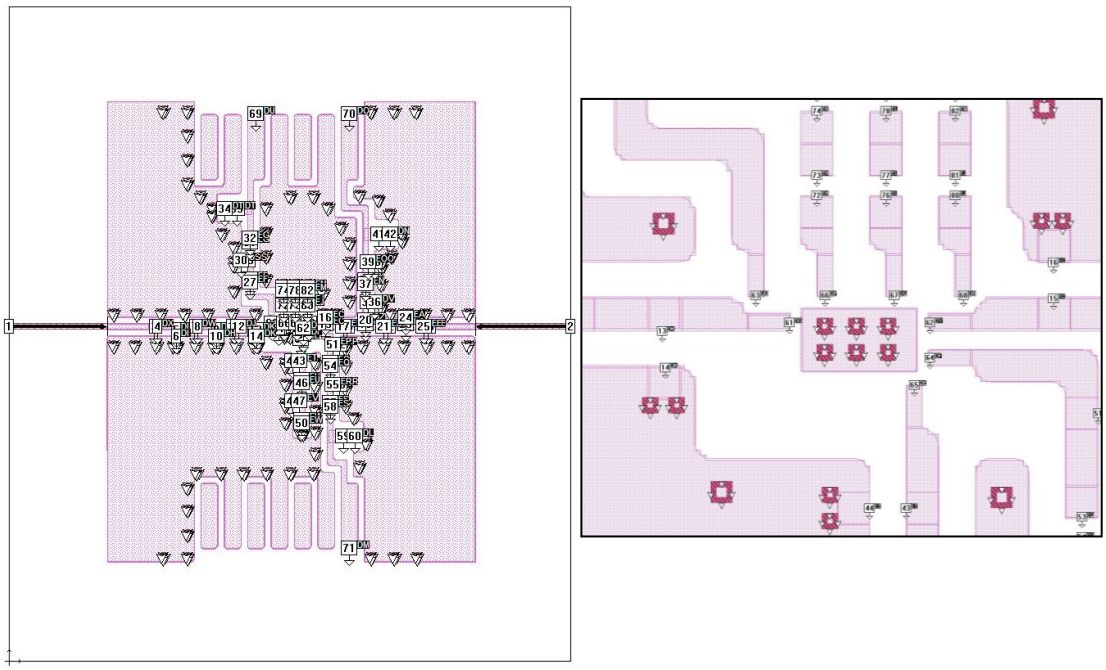

Figure 3.62: Sonnet.geo simulation model of Testboard_2

Sonnet™ is the electromagnetic (EM) simulator used to get an accurate characterization of the testboard. In an EM simulation, the circuit is divided into a fine grid of cells and require a large matrix to formulate the solutions. A cell size of 0.1 mm X 0.1 mm is used. The metal layer is set to Copper with a conductivity of 0.058 GS/m and the dielectric is Rogers 4350 (ε_r = 3.48) with a substrate height of 0.254 mm. Figs. 3.61 and 3.62 are the screenshots for Testboard_1 and Testboard_2, respectively.

The right diagrams of Figs. 3.61 and 3.62 are enlarged views of the testboards that show the pad location for the MMIC. The output files for the EM simulations are S-parameter files that are used in ADS. EM simulations were performed to get more accurate results since the testboard effects such as its losses and coupling are now taken into account. The comparison of S-parameter results with and without the testboard effects simulated in Sonnet are shown in Figs. 3.63 to 3.65. These are taken from the baseline for DA1B. From the figures, it is obvious that with the addition of the Sonnet data, the simulation gets closer to the measured results. For S_{21} (gain) at 1.7 GHz, the difference between measured and simulated results without the sonnet data is about 3 dB compared to only 0.08 dB when the losses due to the testboard are included.

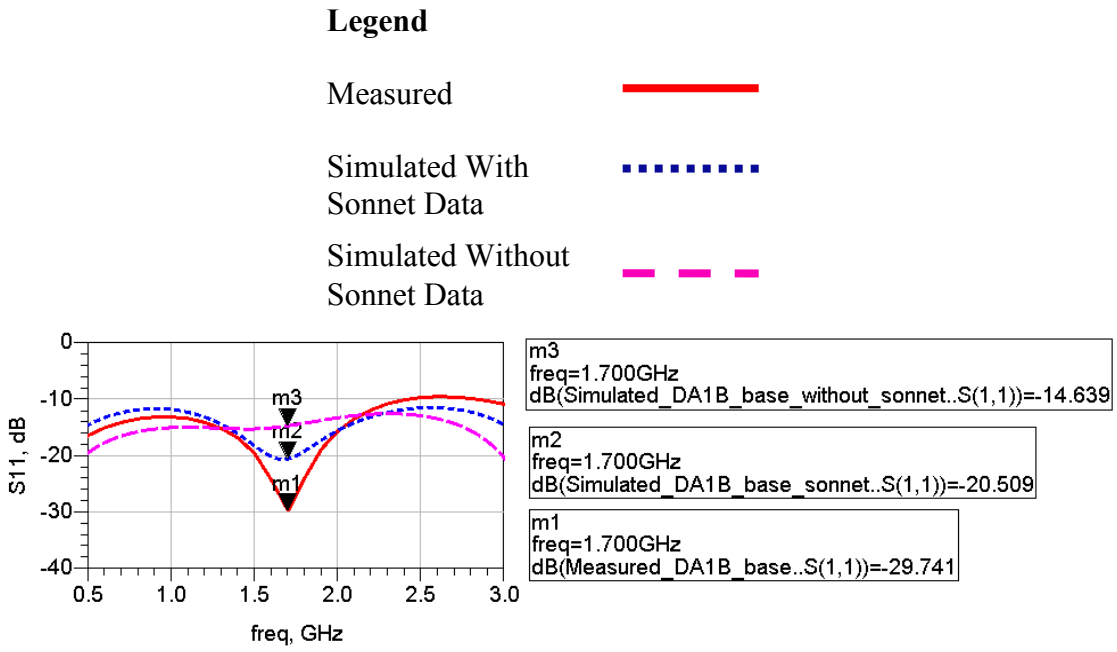

Figure 3.63: S_{11} results for DA1B baseline with and without Sonnet data

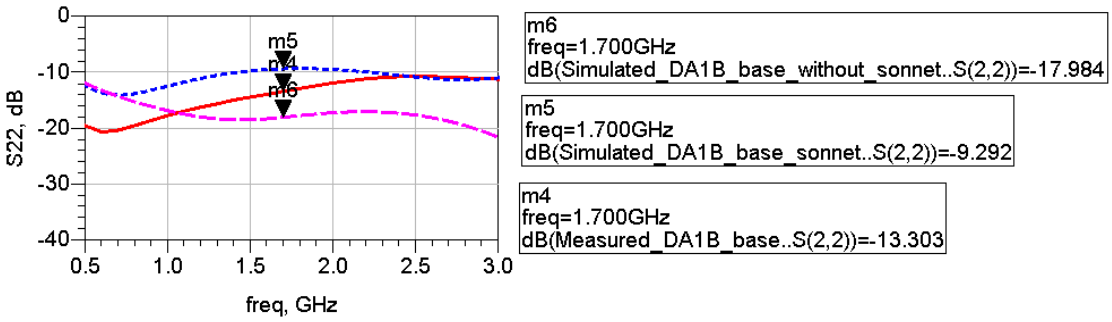

Figure 3.64: S_{22} results for DA1B baseline with and without Sonnet data

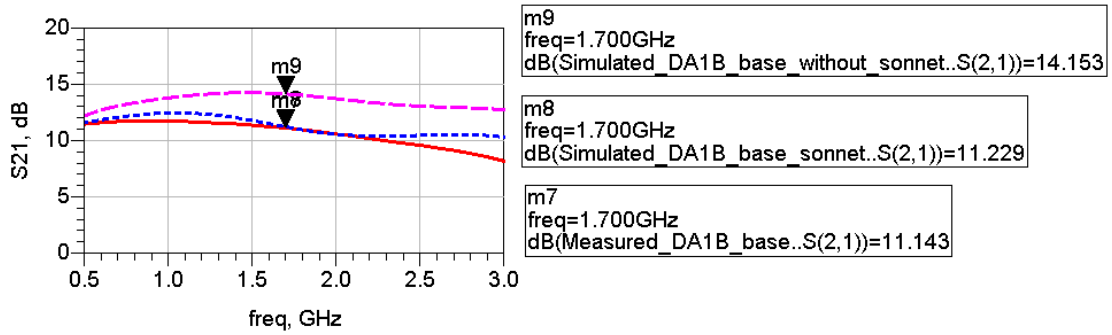

Figure 3.65: S_{21} results for DA1B baseline with and without Sonnet data

3.12.3 Stability Simulation Setup

Stability of the amplifier is a very important condition that must be satisfied before other parameters such as output power and linearity can be taken into account. When oscillations occur, the active device is pushed into its large signal mode and the performance changes very significantly. The small signal S-parameters will not be valid and the amplifier will not function as designed.

For unconditional stability to be achieved, the Rollet Stabilty Criterion (k-factor) or Edwards-Sinsky Stability Criterion (μ-factor) must be more than unity. The k-factor assures unconditional stability but does not provide a relative measure of stability. Edwards and Sinsky [136] developed the μ-factor stability criterion with unconditional stability given as

$$\mu = \frac{1-|S_{11}|^2}{|S_{22}-S_{11}^{*}\Delta|+|S_{21}S_{12}|} > 1 \tag{3.47}$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.48}$$

Larger values of μ indicate greater stability and the μ-factor is the single sufficient condition for unconditional stability in comparison with the k-factor which needs two. For the k-factor analysis, unconditional stability occurs when k is more than unity and magnitude of the determinant, $|\Delta|$ is less than 1. Stability factor, k is calculated by:

$$k = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} \tag{3.49}$$

The simulated μ-factors for the DAs in ADS are shown in Appendix B. From Table C.1 to C.7, the all the amplifier designs are stable before and after adding the LC trap. The μ-factor is more than unity indicating unconditional stability. As mentioned in Section 2.9.6, the addition of the traps can cause instability if not properly designed. From the results in Appendix B, the μ-factor is lowered after the addition of the traps. Nevertheless, the μ-factor for all the variants still remain above unity even after adding the LC traps so unconditional stability is still maintained.

For circuits where the LC traps placed at the input of the HBT (DA1A, DA1B and DA4A), the C_{bypass} plays a role in maintaining unconditional stability when the traps are added. If the C_{bypass} is removed (shown in Fig. 3.66), the μ-factor drops below unity from 40 MHz to 200 MHz for DA1B when the traps are added. The simulation results are shown in Table 3.15.

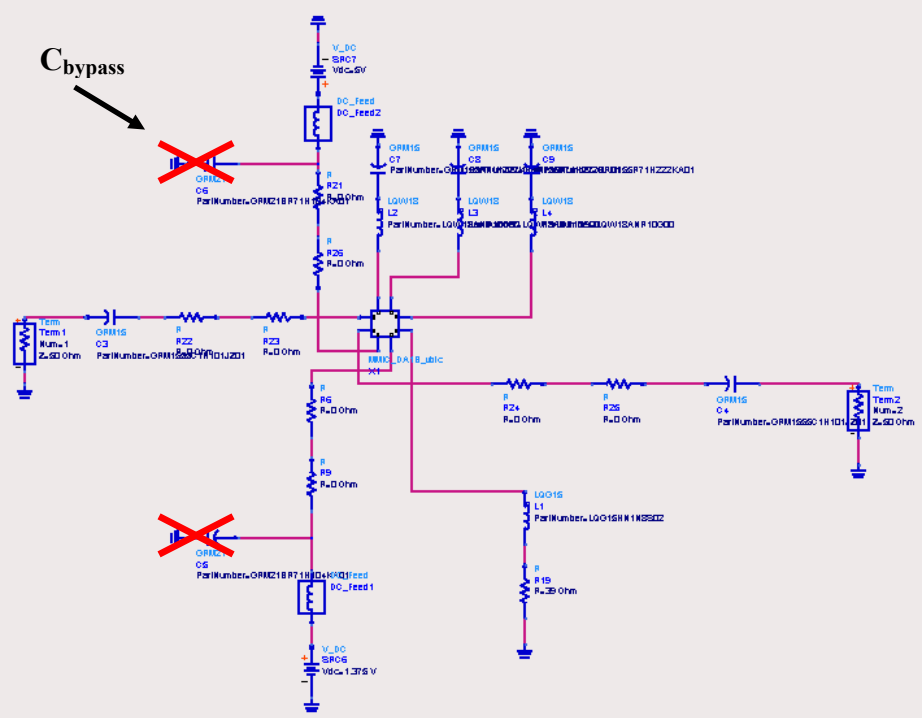

Figure 3.66: DA1B circuit schematic without C_{bypass}

Table 3.15: μ-factor for DA1B (with LC trap) with and without C_{bypass}

freq	DA1B_trap_stability..Mu1	DA1B_trap_without_Cbypass..Mu1
10.00 MHz	1.029	1.087
20.00 MHz	1.103	1.049
30.00 MHz	1.195	1.012
40.00 MHz	1.282	0.969
50.00 MHz	1.358	0.921
60.00 MHz	1.422	0.869
70.00 MHz	1.476	0.815
80.00 MHz	1.520	0.761
90.00 MHz	1.557	0.709
100.0 MHz	1.588	0.662
200.0 MHz	1.723	0.878
300.0 MHz	2.257	1.701
400.0 MHz	3.911	2.536
500.0 MHz	5.847	3.200
600.0 MHz	7.871	3.685
700.0 MHz	9.538	3.967
800.0 MHz	11.001	4.160
900.0 MHz	11.957	4.299
1.000 GHz	12.562	4.452
1.100 GHz	12.412	4.627
1.200 GHz	11.618	4.841
1.300 GHz	10.494	5.101
1.400 GHz	9.396	5.422
1.500 GHz	8.511	5.806
1.600 GHz	7.829	6.261
1.700 GHz	7.358	6.802
1.800 GHz	7.044	7.450
1.900 GHz	6.883	8.213
2.000 GHz	6.835	9.109
2.100 GHz	6.910	10.108
2.200 GHz	7.094	11.170
2.300 GHz	7.399	11.982
2.400 GHz	7.811	12.067
2.500 GHz	8.326	11.362
2.600 GHz	8.834	10.616
2.700 GHz	9.017	10.061
2.800 GHz	8.583	9.690
2.900 GHz	7.818	9.386
3.000 GHz	7.123	9.057

μ-factor <1

3.12.4 S-parameter Simulation Setup

Fig. 3.67 shows how the small signal S-parameters simulation is performed in ADS. The s83p file (input to the testboard data item block) from the EM simulation in Sonnet is used together with the MMIC DA circuit. The schematic for the MMICs have already been shown in Figs. 3.8, 3.9, 3.29, and 3.30. There is also an enlarged view of the simulation parameters.

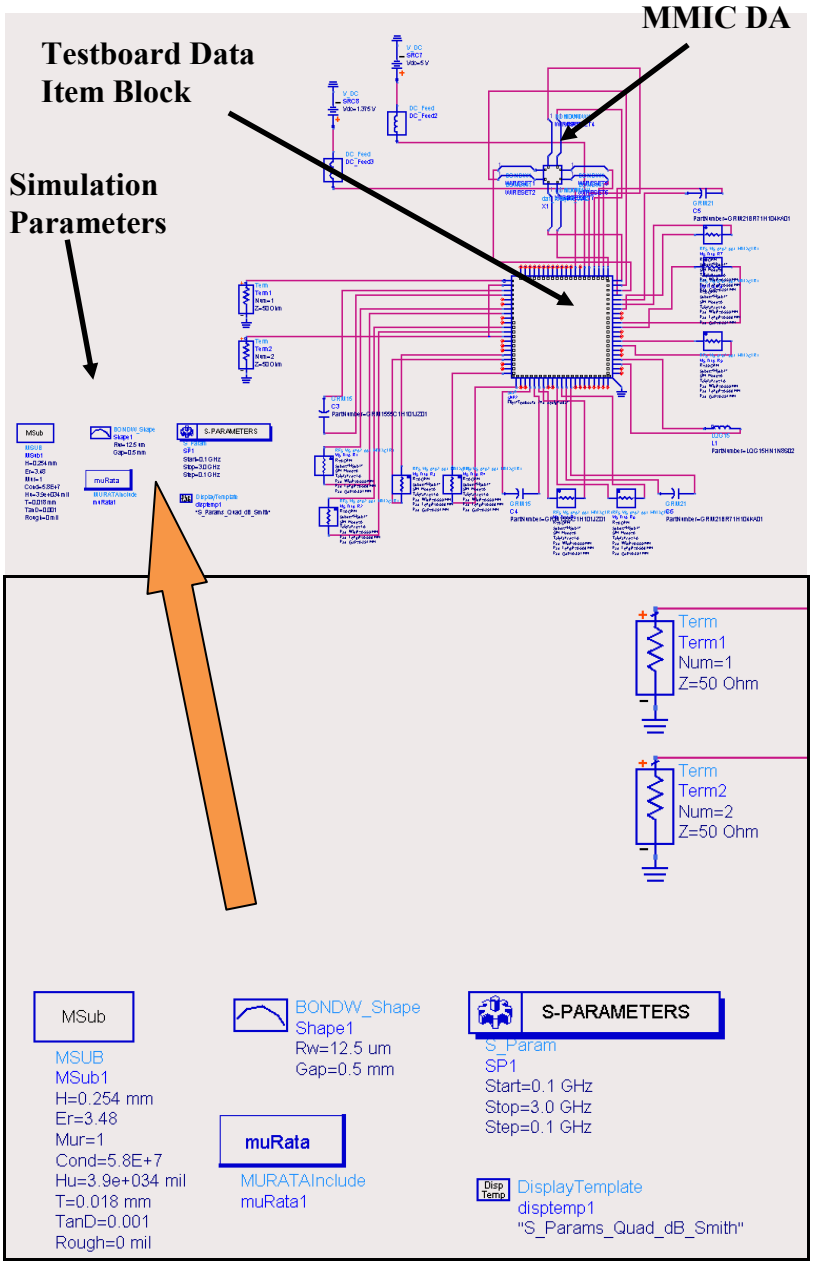

Figure 3.67: S-parameters simulation screenshot in ADS

The MSub definition used in ADS is based on the testboard design explained earlier in Section 3.4. Bondwire effects are also simulated. The bondwires are 1 mil in diameter (≈ 12.5 μm in radius) and the distance from the bondpad to the runner is about 0.5 mm. S-parameters are simulated from 0.1 GHz to 3.0 GHz for the DAs. The ports on the testboard data item block correspond to the ports defined in the Sonnet simulation (See Figs. 3.61 and 3.62). The Murata and Modelithics™ SMT components are connected to the ports based on their locations on the testboard.

3.12.5 P_{1dB} Simulation Setup

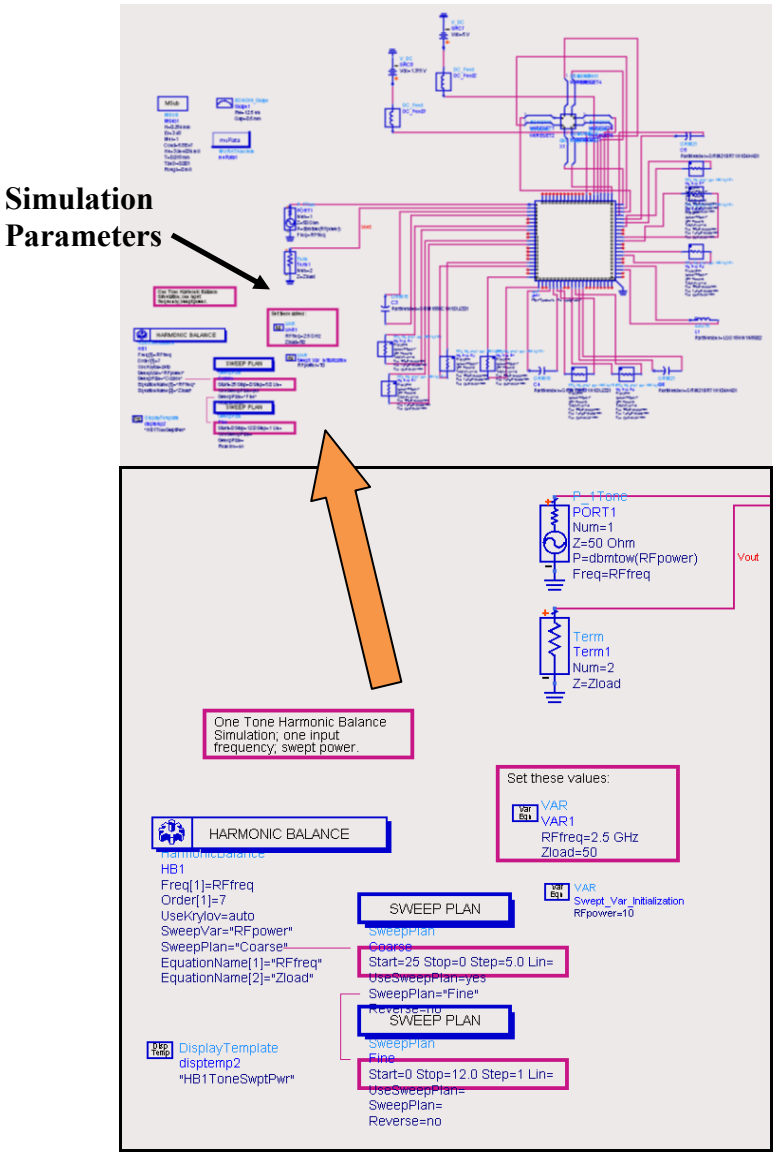

Figure 3.68: P_{1dB} simulation screenshot in ADS

For large-signal simulations, the harmonic balance simulator is used. Harmonic balance calculates a circuit's steady state response and is applicable for a wide variety of problems in microwave circuits such as power amplifiers and mixers. P_{1dB} is the output power when the gain is compressed by 1 dB. So, the frequency must be fixed and the single tone input power is swept until the gain compresses by 1 dB as shown in Fig. 3.68. The simulations were performed from 0.5 GHz to 3.0 GHz at 0.5 GHz intervals. The input power sweep plan is firstly at 5 dBm steps from -25 dBm to 0 dBm and then at 1 dBm steps from 0 dBm to 12 dBm.

Fig. 3.69 shows the results for P_{1dB} simulation at 2.5 GHz and it is clear that with the gain compressed by 1 dB, the output power is 19.92 dBm which is the P_{1dB} of the amplifier. The input power that results in P_{1dB} is around 10 dBm (indicated by marker 3). So OIP3 measurements must be taken at an input power of at least 12 dB backed off from 10 dBm.

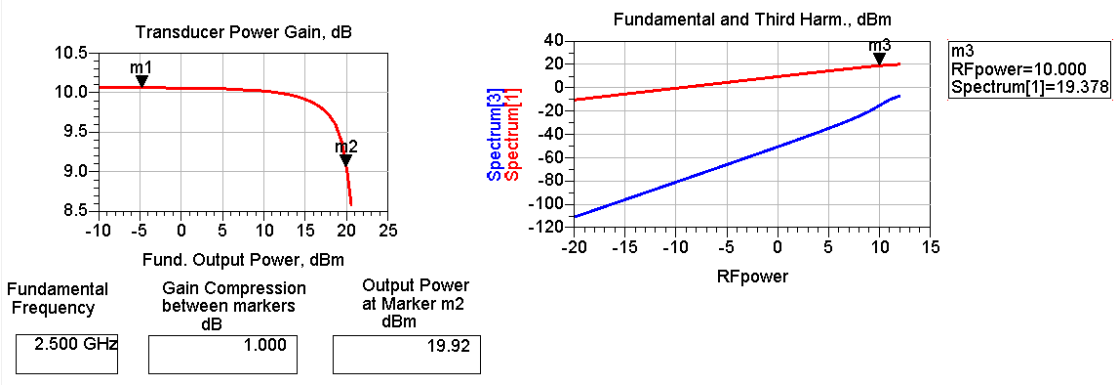

Figure 3.69: P_{1dB} simulation results of DA1B baseline at 2.5 GHz in ADS

3.12.6 OIP3 Simulation

OIP3 (linearity) simulations uses two tones at -5 dBm input power (at least 12 dB backed from the Pin that results in P_{1dB}). The reason for this is to ensure that the amplifier is operating in the "linear" region and it is normally where the amplifier will be operated. The simulations were also performed from 0.5 GHz to 3.0 GHz at 0.5 GHz intervals. A spacing of 10 MHz between the two input signals is used. The screenshot for the OIP3 simulations is shown in Fig. 3.70.

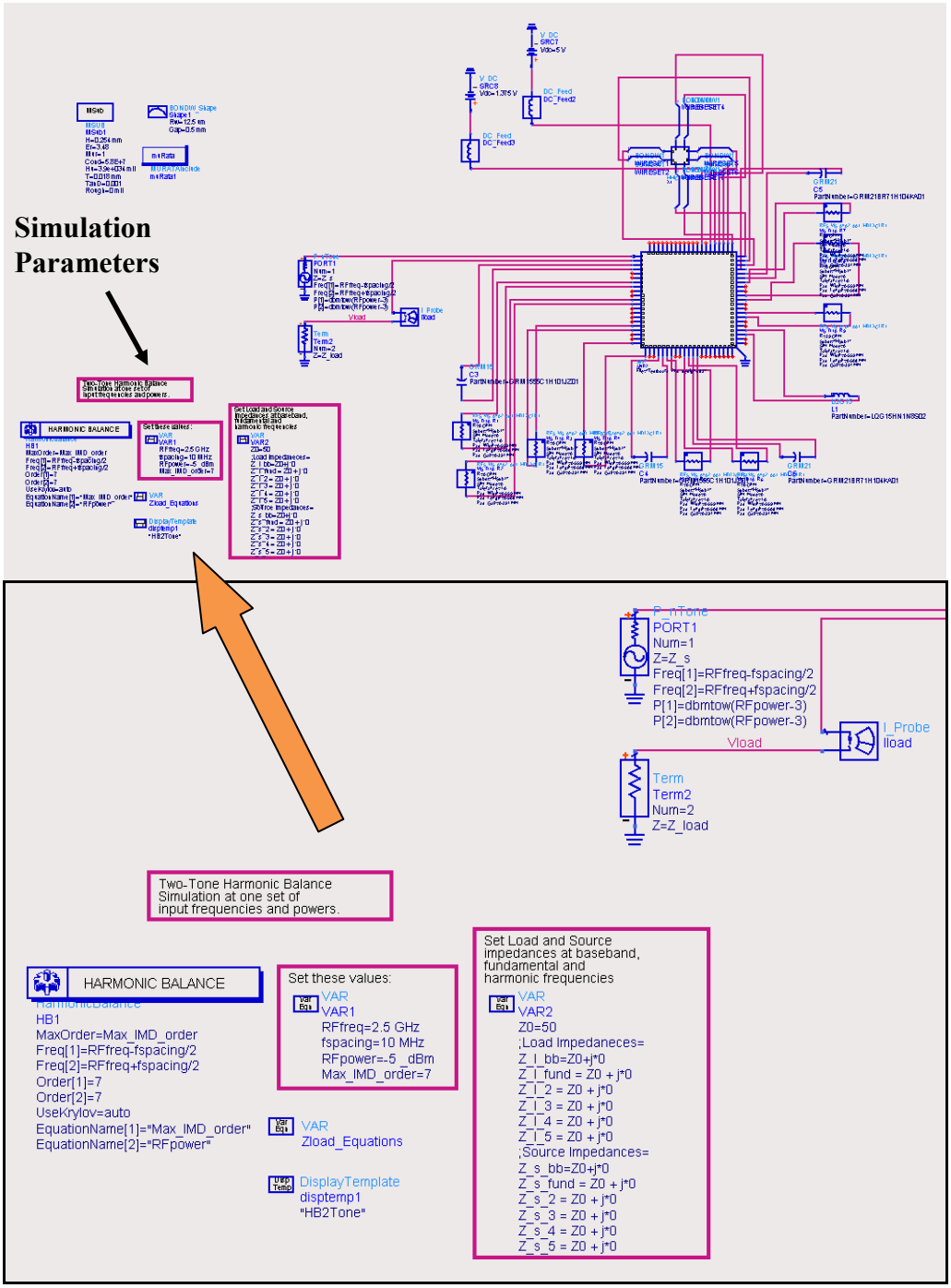

Figure 3.70: OIP3 simulation screenshot in ADS

Fig. 3.71 shows the results of the OIP3 simulation. From the output spectrum, OIP3 = $P_o + (P_o - P_3)/2$. This calculation is done for both the left and the right output tones resulting in the low and high side OIP3. The lower value is taken as the OIP3 of the amplifier. In this simulation, the OIP3 is 30.306 dBm. Sometimes, the linearity for amplifiers especially LNAs are stated as the Input Third Order Intercept Point (IIP3).

The IIP3 = OIP3 – Transducer Power Gain. As shown at the bottom of the results screenshot, the results become invalid as the amplifier is driven into compression. Therefore, the input power into the amplifier is set to -5 dBm where it is sufficiently backed off, ensuring the amplifier is operating in the "linear" region.

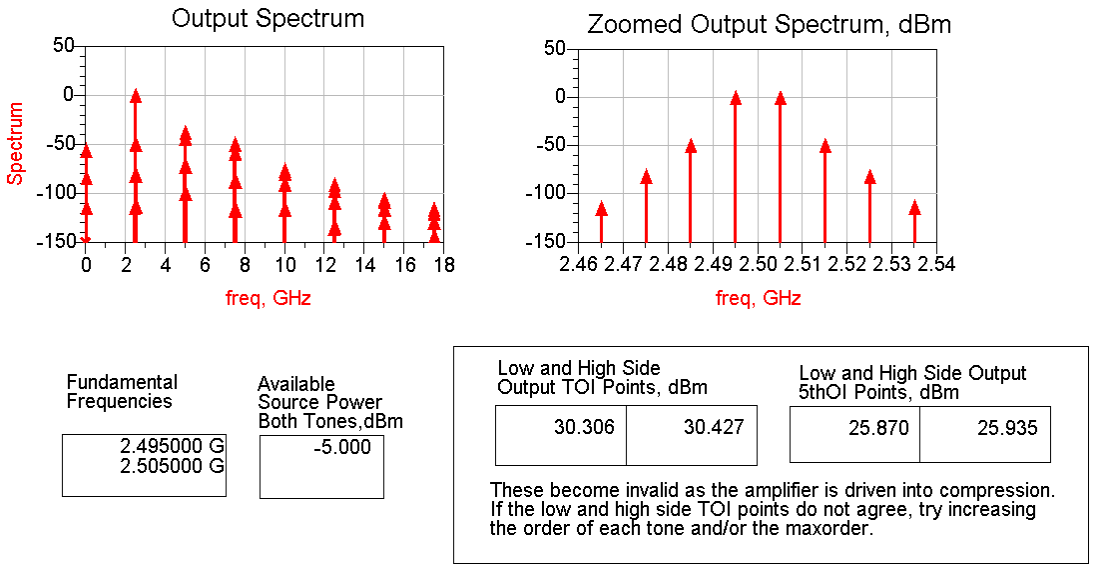

Figure 3.71: OIP3 simulation results of DA1B baseline at 2.5 GHz in ADS

3.13 Measurement Setup

In this section, an explanation of how the measurement results are obtained using the equipment listed in Table 3.16 is given. Measurements were performed at Mini-Circuits Technologies (M) Sdn. Bhd. in Penang. Before the small and large signal measurements are performed, the input of the DA is terminated with a 50 Ω termination with no input signal and the output spectrum is analyzed for the existence of output intermodulation spurs. The presence of spurs indicates instability. Nevertheless, the DAs for the first and second design are stable since they have been designed for unconditional stability. This is true even with the addition of the LC traps. The measurements are performed at least three times to determine that they are in agreement with each other.

Table 3.16: List of Equipments for measurements

Equipment	Model	Manufacturer	Description
Network Analyzer	N3383A	Agilent	300 kHz – 9 GHz PNA Series
Electronic Calibration Module	N4691-60001	Agilent	10 MHz – 26.5 GHz Cal Kit
DC Power Supply	E3631A	Agilent	0 – 6 V, 5A / +/- 25 V, 1A Triple Output
Spectrum Analyzer	N9020A	Agilent	20 Hz – 13.6 GHz MXA Series
Signal Generator	N5181A	Agilent	100 kHz – 6 GHz MXG Series
Attenuator (20 dB)	BW-S20W2+	Mini-Circuits Labs	2W, DC – 18 GHz, 20 dB Pad
Power Splitter / Combiner	ZN2PD2-63-S+	Mini-Circuits Labs	350 – 6000 MHz

3.13.1 S-parameter Measurement Setup

Figs. 3.72 and 3.73 indicate how the Device Under Test (DUT) is connected to the Network Analyzer for small signal measurements. The DUT is the MMIC DA wirebonded to the testboards. Before measurements can be made, the network analyzer together with the cables must be calibrated. This is to set the reference plane at the DUT itself. The calibration is done using the N4691-60001 Electronic Calibration Module. S-parameter measurements are obtained from 0.1 GHz to 3 GHz and the data is saved using the s2p (Touchstone) file format.

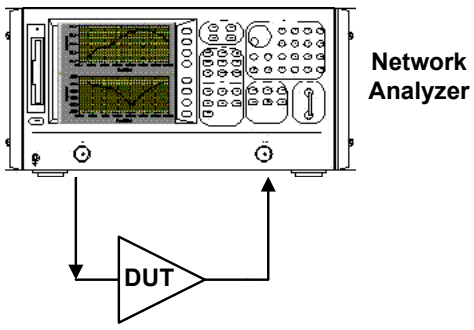

Figure 3.72: S-parameter measurement setup (descriptive)

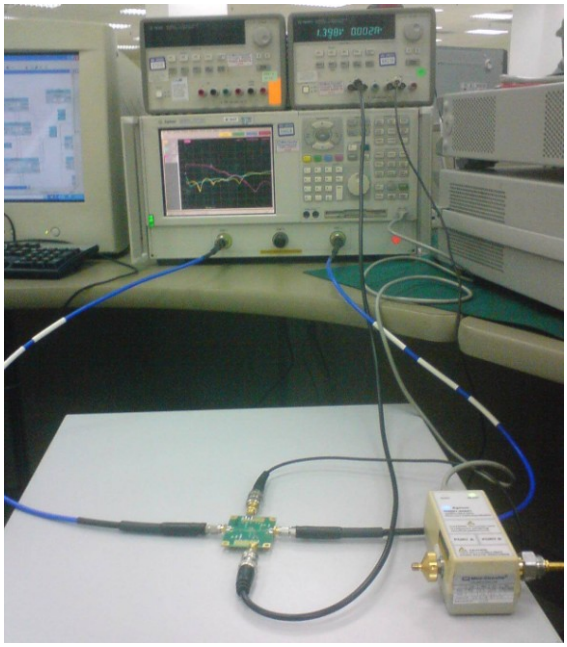

Figure 3.73: S-parameter measurement setup (actual)

3.13.2 P_{1dB} Measurement Setup

Figs. 3.74 and 3.75 show the block diagram and actual P_{1dB} measurement setup. Cable losses are first taken into account by using the E4418B Power Meter. A DC block is necessary because the Spectrum Analyzer cannot sink DC current. A 20 dB attenuator (pad) is fixed to ensure the amplified power does not exceed 1W (maximum input power to Spectrum Analyzer). Input power from the signal generator is increased from -20 dBm to 12 dBm and the output power is recorded using the Spectrum Analyzer.

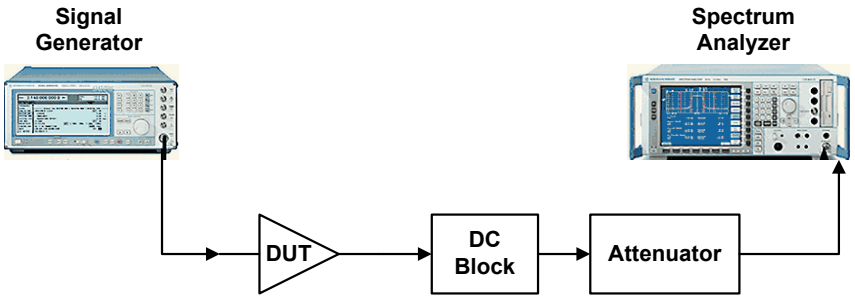

Figure 3.74: P_{1dB} measurement setup (descriptive)

Figure 3.75: P_{1dB} measurement setup (actual)

Fig. 3.76 shows the results from P_{1dB} measurements at 2.5 GHz for the DA1B baseline. From these results, the P_{1dB} is 20.02 dBm (output power when gain has dropped 1 dB). This is close to the simulated value of 19.92 dBm (in Section 3.12.5).

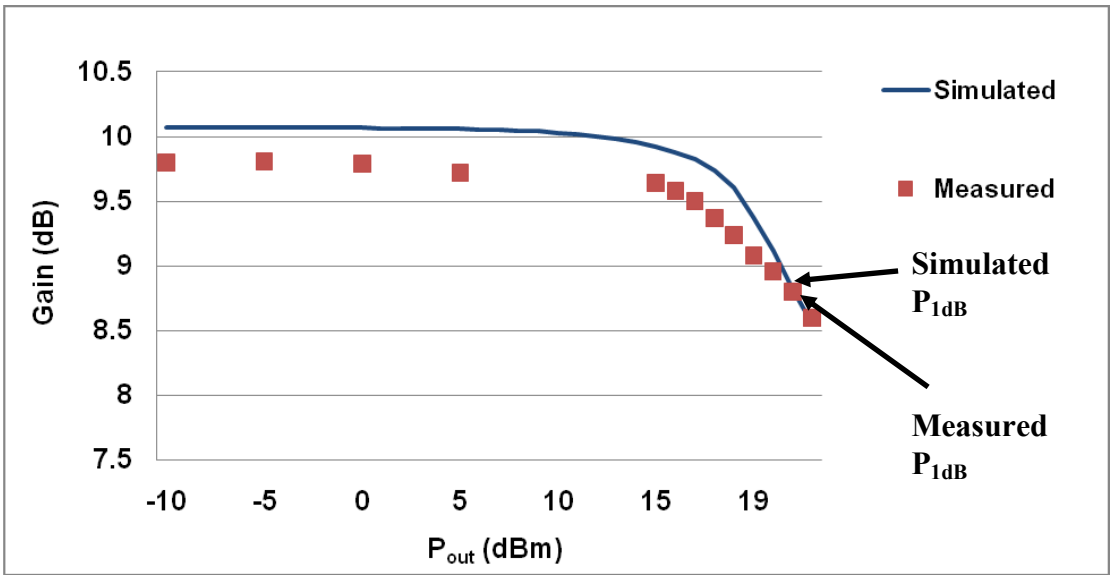

Figure 3.76: Measured and simulated Gain versus P_{out} results for DA1B baseline at 2.5 GHz

3.13.3 OIP3 Measurement Setup

For OIP3 measurements, two signals at -5 dBm are combined and input to the DUT. The frequencies of the input signals are spaced 10 MHz and the output spectrum is viewed on the Spectrum Analyzer. The output power of the fundamental tone and third order tone are recorded. Isolators are used to force the signal from the generator to travel only in the forward direction. This will ensure the intermodulation distortion is only from the DUT and not sourced from the generators. Mica Microwave isolators model T-601S01 (minimum isolation of 17 dB) and T-602S01 (minimum isolation 20 dB) were used in the measurements. The descriptive (block diagram) and actual setups for OIP3 are shown in Figs. 3.77 and 3.78.

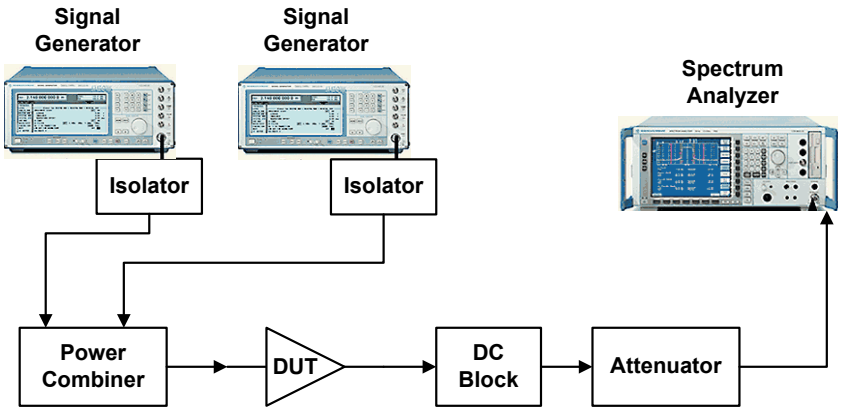

Figure 3.77: OIP3 measurement setup (descriptive)

Figure 3.78: OIP3 measurement setup (actual)

For example, to measure the OIP3 at 2.5 GHz, the first tone, f_1 is at 2.495 GHz and the other is at f_2 is at 2.505 GHz (spacing of 10 MHz). Fig. 3.79 shows the output spectrum with a span of 100 MHz. The results for DA1B at 2.5 GHz are shown in Table 3.17. The DA at baseline and with 2.2 nF and 100 nH trap are shown with the power obtained at each respective frequency. After taking into account the cable loss, the OIP3 for the low side and high side are calculated (based on equation (2.12)). The actual OIP3 would be the lower value between the low and high side OIP3. Recall that the simulated OIP3 for the baseline (in Section 3.12.6) is 30.306 dBm, close to the measured value of 31.78 dBm.

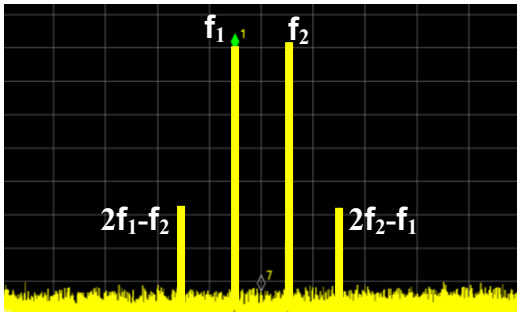

Figure 3.79: Output spectrum at spectrum analyzer with span 100 MHz

Table 3.17: Measured OIP3 results for DA1B at 2.5 GHz

DA1B	$2f_1-f_2$ (dBm)	f_1 (dBm)	f_2 (dBm)	$2f_2-f_1$ (dBm)	Loss (dB)	OIP3 Low (dBm)	OIP3 High (dBm)	OIP3 (dBm)
Base	-72.13	-16.95	-17.08	-72.54	21.14	31.78	31.79	31.78
Trap	-86.74	-16.89	-17.02	-87.68	21.14	39.18	39.45	39.18

Figure 3.80: Data collection at Mini-Circuits Technologies, Penang

3.14 Measurement Verification

Calibration is an important step that must be performed before measurements can be made. It involves measuring known standards and using those measurements to compensate for losses, mismatches or feedthroughs. The network analyzer has connectors at the front panel but there are test cables which connect them to a device under test (distributed amplifier). These cables will introduce a time delay and phase shift as well as losses to the measurements. By performing calibration, the reference planes are set at the input and output ports of the DUT, resulting in accurate measurements. For the Agilent N3383A Network Analyzer, calibration is done using the N4691-60001 Electronic Calibration Module (ECal). By using the ECal, calibration need not be performed using the traditional mechanical tools thus saving time and effort.

A full two port calibration was performed with the ECal. Typical full two port calibration usually involves three impedance standards (short open and load) and one transmission standard (thru) and therefore is known as the SOLT calibration. However, even after using the ECal to perform the calibration, it is an important to verify the calibration by performing verification steps.

To verify the calibration, the three impedance standards from the mechanical calibration kit are attached to both ports and its response is viewed on the Network Analyzer via the Smith chart. The correct S-parameter response on Smith chart when the short, open and load (50 Ω) standards are attached to the port is shown in Fig. 3.81. If the calibration using the ECal is done correctly, the results on the Smith chart when the mechanical calibration standards are attached should be the same as Fig. 3.81. When the transmission standard (thru) is attached between port 1 and port 2, the S_{21} response should be close to 0 dB. The calibration is verified to be indeed correct and the error for S_{21} when the thru standard is attached between both ports of the Network Analyzer is within +/- 0.05 dB.

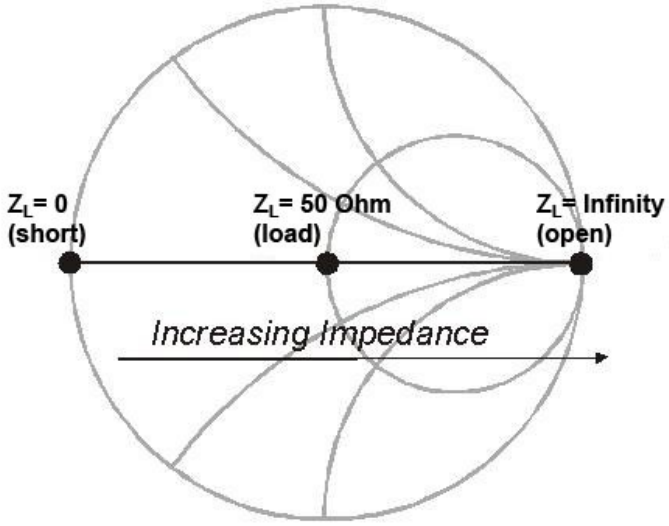

Figure 3.81: Locations of short, open and load (50 Ω) on Smith chart

Verification of the power generated from the Signal Generator is accomplished by checking it with the Agilent E4418B Power Meter. For the Spectrum Analyzer, its output is verified by connecting it to the Signal Generator. By varying the output power and frequency of the signal from the Signal Generator, these results should be accurately displayed on the Spectrum Analyzer. In my measurements, the frequency of the signal can be accurately determined by the S.A. since the 10 MHz reference ports of the Signal Generator and S.A. are both connected together. The error in power levels after taking into account the losses from the attenuator and connectors is within +/- 0.02 dB.

The measurements were taken with the MMIC die-attached onto the testboards so the calibration does not de-embed the parasitics of the testboard. The de-embedding is right up to the SMA connectors on the testboard. The only alternative for measuring the MMIC directly is by using a probe station but this makes it hard to add the external LC traps. Besides, prototype measurements performed in companies are mostly done with a testboard since the final product will be the die attached to a package and used in a testboard environment.

3.15 Summary

This chapter explains in detail the steps and considerations taken in designing the DA. Two design iterations for the DA were made to test the LC traps. The first design iteration has four variants and was used to test the effects of the traps at the output whereas the second design iteration has three variants and was made to examine traps at the input of the HBT. The reason a second design iteration is necessary is because modifications needed to be made to include bond pads that go directly to the input of the HBT. The schematic and layout of the MMIC were performed using the ADS software. The dies for the first design iteration were fabricated using the WIN H02U-41 InGaP/GaAs HBT foundry process and had a dimension of 2020 μm X 660 μm. The variants for the designs differ in terms of the stabilization resistor and equalization capacitor values. The dies for the second design iteration were fabricated using the WIN H02-43 process. The size of the MMIC is 1620 μm X 660 μm.

Testboards which act as a platform for measurement data to be collected were also designed using AutoCAD. Two iterations were also made and both are 40 mm X 50 mm in dimensions. These testboards uses grounded CPW as its transmission media and has three metal layers with the Rogers 4350 dielectric and FR4 as the support material. Chapter 3 also includes an account of how the die-attach, wire-bonding and board population of SMTs were performed.

An analysis of the relationship between the low impedance terminations to linearity of the HBTs shows that the third order output current, $I_{o,2\omega 2-\omega 1}$ depends on the second order base-collector voltage, V_{bc} at frequencies $2\omega_2$ and $\omega_2-\omega_1$. Although placing a trap at the output tunes the V_{ce}, but C_{bc} is a nonlinear capacitance dependent on V_{ce}. Another analysis also shows that third order output current is dependent on the base-emitter voltage at the envelope frequency, $V_{be,\omega 2-\omega 1}$. By placing traps at the input to provide low impedance at the envelope frequency, the $Z_{S,\omega 2-\omega 1}$ as can be reduced. This will cause the $V_{be,\omega 2-\omega 1}$ and ultimately the $I_{o,2\omega 2-\omega 1}$ to drop. Third order output currents are dependent on the input impedance at the second harmonic, $Z_{S,2\omega 2}$ as well. However, tuning for the second harmonic is not feasible for a broadband application and will be disregarded since it will affect the in-band response of the DA.

This chapter also explains the simulation and measurement setup as well as the verification steps taken to ensure the measured data is accurate. To provide accurate simulation results, the testboards effects are taken into account by using the Sonnet™ electromagnetic simulator. The SMT components models from Modelithics™ provide a better characterization of the behaviour for these components past their series resonance frequency (SRF). The HBT models are from WIN Semiconductor and the simulations were performed using ADS. The S-parameters, P_{1dB} and the OIP3 for the DA with and without the presence of the traps were measured. S-parameter results are the small-signal response of the DA. P_{1dB} is obtained by doing a power sweep while maintaining frequency whereas the OIP3 is obtained from the two tone measurements with closely spaced frequencies. Even after performing calibration using the electronic calibration unit, the measurements were verified using the mechanical calibration kit to ensure that the data collected is indeed accurate.

CHAPTER 4
RESULTS AND DISCUSSION

4.1 Introduction

Results from placing the LC trap at the input and output of the HBT are shown and discussed in this chapter. Results from Section 4.2 have been accepted for publication at the International Conference on Intelligent and Advanced Systems, (ICIAS) in Kuala Lumpur [14] while results from Section 4.3 have been accepted for publication at the European Microwave Conference (EuMC) in Paris [15].

4.2 Results from Implementing LC trap at Output of HBT

The first iteration of DA designs are measured with and without the LC trap located at the output of the HBT. Refer to Section 3.2.6 for location of the LC trap at the output. The first DA designs are DA1, DA2, DA3 and DA4. In the following subsections, the results shown are with the LC trap values of 2.2 nF and 100 nH, unless specified, otherwise. The base bias voltage, V_{be} is 1.375 V and the collector bias voltage, V_{ce} is 5 V. The results in this section have been accepted for publication at the International Conference on Intelligent and Advanced Systems, (ICIAS) in Kuala Lumpur [14].

4.2.1 S-parameter Results

Although impedance and admittance parameters are commonly used for measuring circuit performance, these measurements are impractical at high frequencies. This is because it is very difficult to implement a short or an open at RF frequencies. Also,

controlling stability is difficult if the active device is terminated in an open or short circuit. Another set of parameters called Scattering Parameters are introduced based on travelling waves that enter and leave an n-port network [62]. For a two port network:

a) S_{11} is the input reflection coefficient when the output is terminated in Z_o
b) S_{21} is the forward transmission coefficient between the Z_o terminations
c) S_{12} is the reverse transmission coefficient between the Z_o terminations
d) S_{22} is the output reflection coefficient when the input is terminated in Z_o

The S_{11} and S_{22} represent the input and output return losses respectively and are an indication of how well input and output ports are matched to 50 Ω. An industry standard for the S_{11} and S_{22} (in the logarithmic scale) is 10 dB or better. This is because the mismatch loss is given by

$$ML = -10\log\left(1-|\Gamma|^2\right) \tag{4.1}$$

where Γ is the reflection coefficient. So a return loss of 10 dB gives a mismatch loss of ≈ 0.5 dB. The better the return loss, the lower the losses due to mismatch will be. Figs. 4.1 to 4.12 show the simulated and measured S-parameters for DA1 to DA4.

The baseline measurements refer to the measurements done without the LC trap. After the LC trap has been added, the measurements are those with the term "with trap". The S-parameter measurements that fall right on top of each other are the measurements with and without the traps. Therefore, the in-band S-parameters are not affected by the usage of the traps and this situation is desirable since gain and return loss are not affected after adding the traps. There is a small discrepancy between the simulated and measured values of about +/- 2 dB (for S_{21}) due to the fabrication process loss and parasitic effects of the HBT. The discrepancy is more for return loss but at -10 dB and -20 dB, the difference in terms of magnitude is only 0.09. The purpose of using four different DAs is to prove that with different variants, the S-parameters are still not affected with the traps.

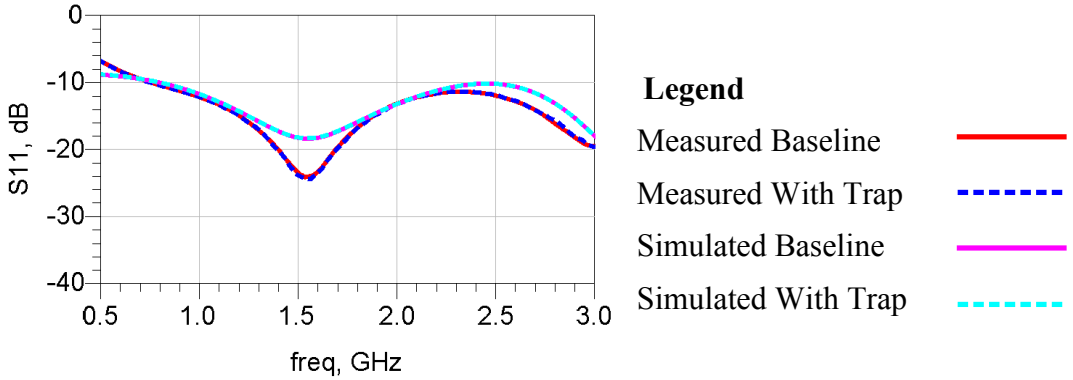

Figure 4.1: S_{11} results for DA1 with and without LC trap

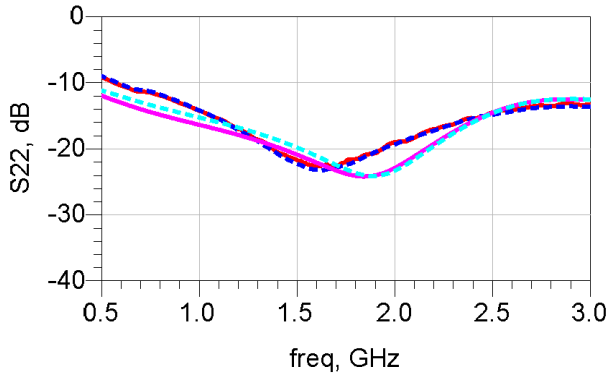

Figure 4.2: S_{22} results for DA1 with and without LC trap

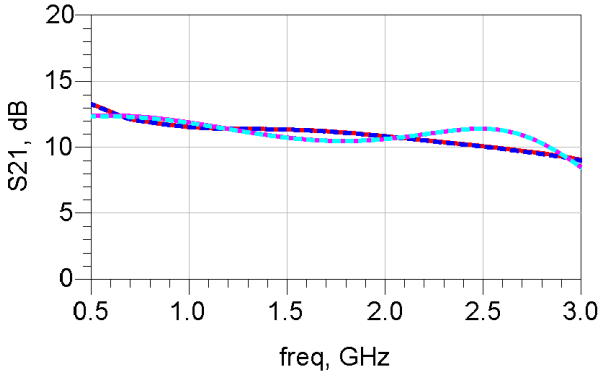

Figure 4.3: S_{21} results for DA1 with and without LC trap

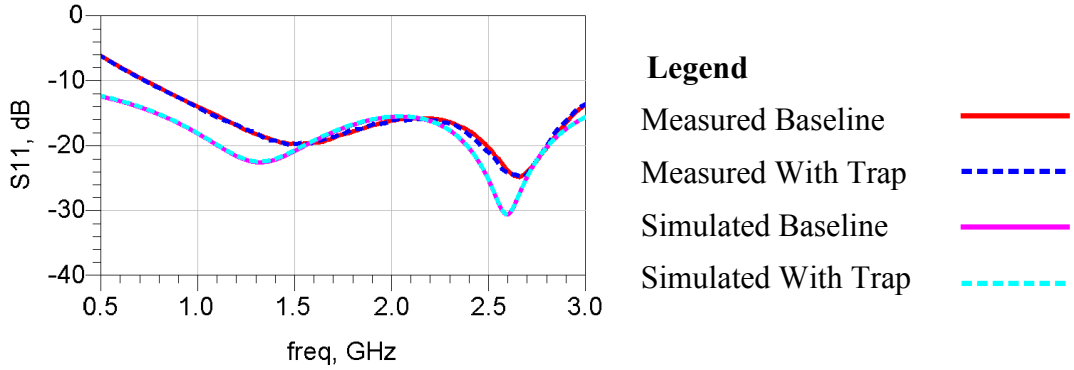

Figure 4.4: S_{11} results for DA2 with and without LC trap

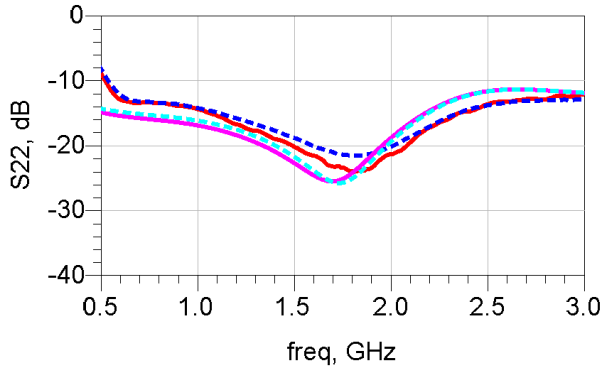

Figure 4.5: S_{22} results for DA2 with and without LC trap

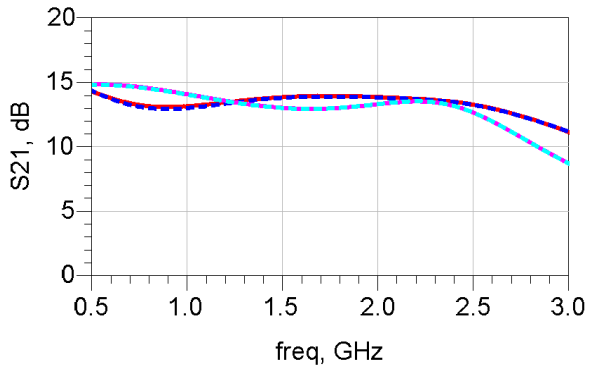

Figure 4.6: S_{21} results for DA2 with and without LC trap

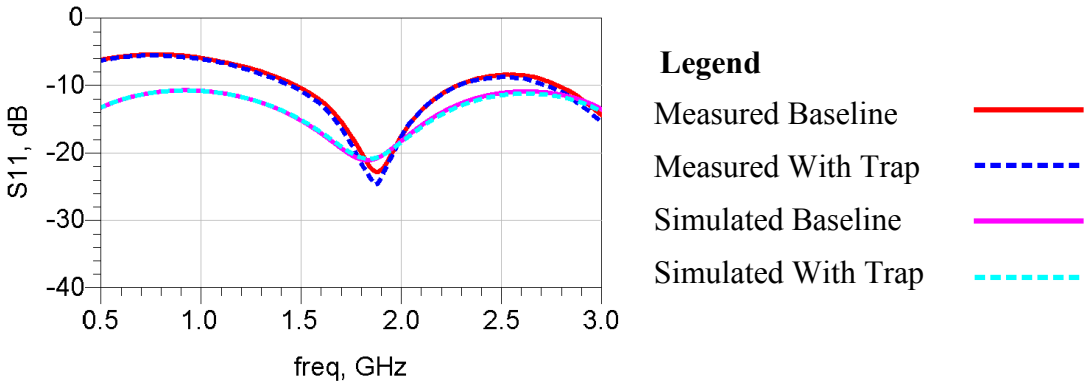

Figure 4.7: S_{11} results for DA3 with and without LC trap

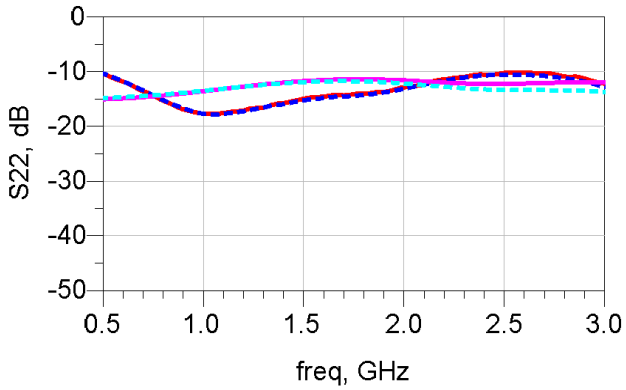

Figure 4.8: S_{22} results for DA3 with and without LC trap

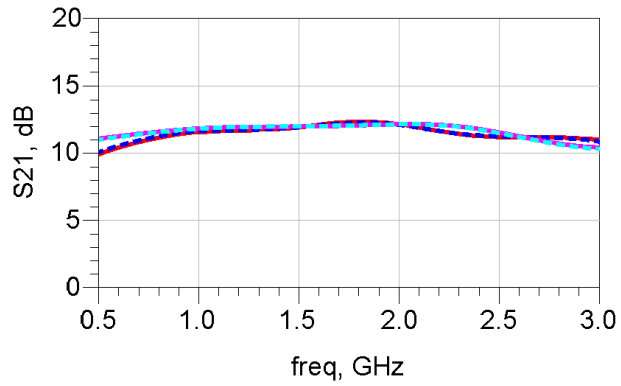

Figure 4.9: S_{21} results for DA3 with and without LC trap

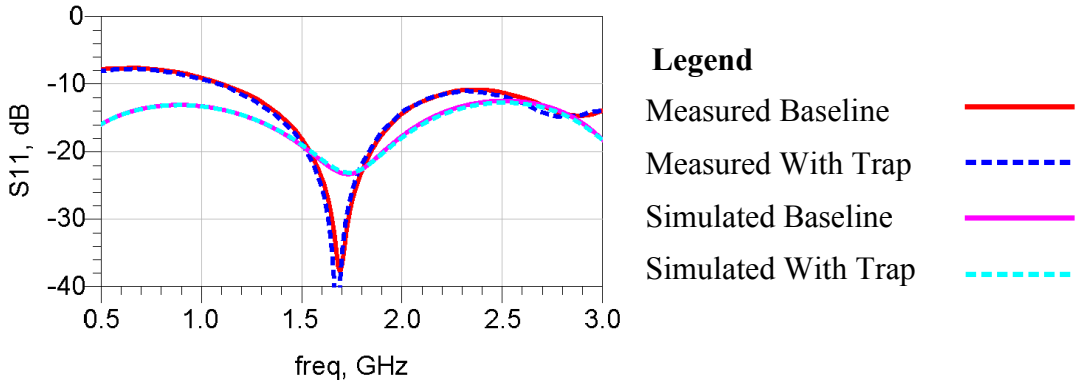

Figure 4.10: S_{11} results for DA4 with and without LC trap

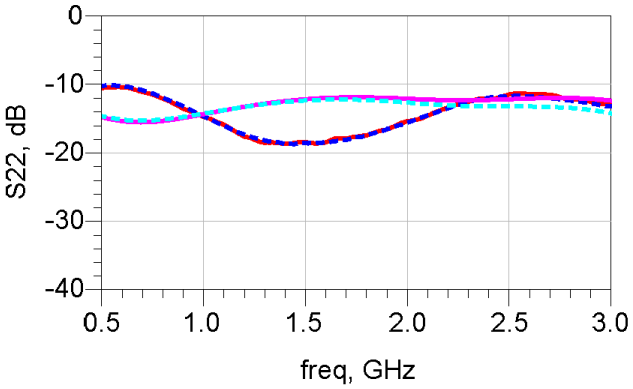

Figure 4.11: S_{22} results for DA4 with and without LC trap

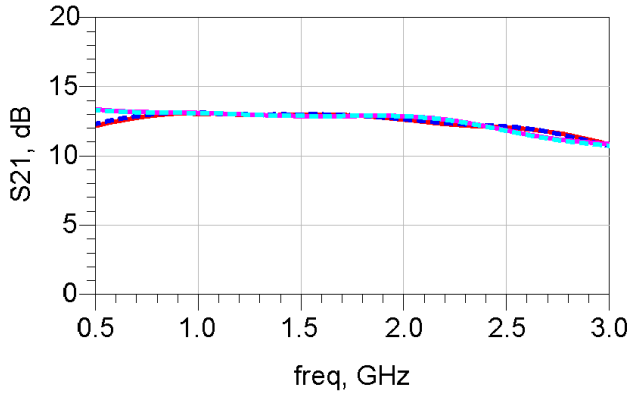

Figure 4.12: S_{21} results for DA4 with and without LC trap

As shown, the trends for the simulated and measured S-parameters agree well. As a rule of thumb, input and output return losses are generally maintained at 10 dB or

better throughout the band of operation (0.5 – 2.5 GHz). The measurements are shown up to 3.0 GHz because OIP3 measurements were taken at that frequency as well. The input return loss (S_{11}) for DA2, DA3 and DA4 is less than 10 dB below 0.5 GHz. (Since it is stated in terms of loss, the negative sign is ignored). However, this helps to maintain a flat S_{21} (gain) throughout the frequency band. Mismatch is introduced to reduce low frequency gain.

For a DA, it is important to maintain the gain variation to within +/- 1.5 dB. The average measured gain is 11.6 dB for DA1, 13.7 dB for DA2, 10.6 dB for DA3 and 12.5 dB for DA4. From the Figures, it is also clear that the LC trap at the output does not affect the in-band S-parameters. This is important because the linearization method should not interfere with the small-signal performance of the amplifier.

For DA2, there are two valleys in the S_{11} as opposed to one for the other three designs due to a resonance at two separate frequencies. DA1 and DA2 differ in terms of the C_{equ} and R_{sta} values. DA2 has a larger C_{equ} of 1.392 pF compared to 0.966 pF for DA1. However, the R_{sta} for DA2 is smaller than DA1. The R_{sta} for DA1 and DA2 are 14.06 Ω and 10.79 Ω, respectively. With different equalization capacitors and stabilizing resistors for DA2, the resonance frequency changes and causes the two valleys shown in Fig. 4.4. Nevertheless, it is not a bad effect since the return loss is maintained to be better than 10 dB.

4.2.2 P_{1dB} Results

The P_{1dB} for the DAs are simulated using ADS and measured using the Agilent N9020A Spectrum Analyzer. The results are compiled and shown in Table 4.1. The simulated results are highlighted in yellow and it is also indicated whether the measurement is the baseline or with the LC trap present at the output. The base bias voltage of 1.375 V puts the amplifier in Class A operation.

From the measured data, the addition of the traps does not affect the P_{1dB} value. The simulated results are close to the measured ones with a maximum discrepancy of 0.88 dB. Increasing the base bias voltage results in more collector current, resulting in

higher P_{1dB}. This is confirmed by comparing the results as the base bias voltage is increased. The measured total collector current is 88 mA for DA1 and DA2, 78 mA for DA3 and 94 mA for DA4.

Table 4.1: P_{1dB} for first design iteration DAs with and without LC trap

DA	Type	P_{1dB} at 1.0 GHz (dBm)	P_{1dB} at 2.0 GHz (dBm)	P_{1dB} at 3.0 GHz (dBm)
DA1	Base (S)	21.20	21.29	18.32
	Base (M)	21.22	21.35	18.76
	Trap (S)	20.71	20.15	19.21
	Trap (M)	20.9	20.91	19.51
DA2	Base (S)	19.21	20.98	19.14
	Base (M)	20.03	21.56	19.3
	Trap (S)	19.22	20.80	19.12
	Trap (M)	19.92	20.90	19.77
DA3	Base (S)	17.47	19.72	17.92
	Base (M)	17.58	19.75	18.02
	Trap (S)	18.97	20.07	21.00
	Trap (M)	18.97	20.74	21.48
DA4	Base (S)	19.83	20.88	20.45
	Base (M)	19.31	21.15	21.00
	Trap (S)	19.83	21.08	21.21
	Trap (M)	19.67	20.70	21.09

Table 4.2 shows the PAE at 2 GHz for DA1 to DA4 at P_{1dB}. As expected, the PAE is less than 25 % since the amplifier is biased at Class A. Adding the traps does not cause a significant effect to the PAE.

Table 4.2: Power Added Efficiency at 2 GHz at P_{1dB} (First design iteration DA)

Type	DA1 (%)	DA2 (%)	DA3 (%)	DA4 (%)
Baseline	21.89	23.90	14.93	13.93
Trap	20.72	23.85	15.78	13.35

4.2.3 OIP3 (Linearity) Results

Comparisons between simulated and measured OIP3 values from the DAs are given. Several parameters are varied to determine the effects of the LC traps to the OIP3 (linearity) of the amplifier. Results will show the linearity with varying inductance of the traps and with different base bias voltages.

4.2.3.1 Simulated versus Measured OIP3

The simulated and measured results for the four DAs are shown in Figs. 4.13 to 4.16. The simulated data are obtained by taking into account the testboard effects using Sonnet™ and by including the SMT models from Modelithics™ in the ADS simulations. The simulated and measured results track well. Placing the low impedance inductor-capacitor network at the output only provides minimal impact on the linearity at the lower frequencies. Only at 2.5 GHz and 3 GHz is there a significant improvement for the OIP3. In fact, for the DAs with series ballasting, the OIP3 with the trap is reduced at 0.5 GHz and 1 GHz.

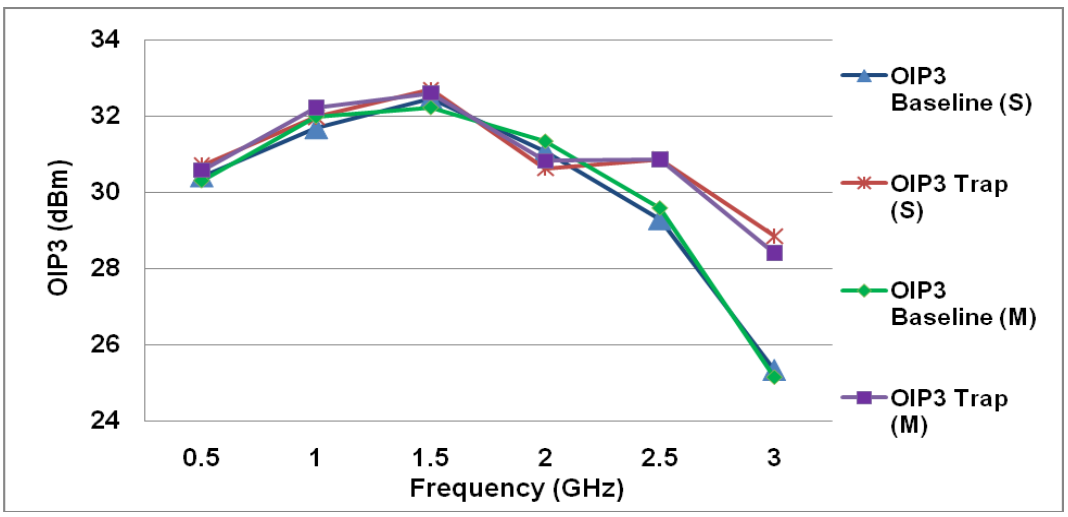

Figure 4.13: Simulated and measured OIP3 results for DA1

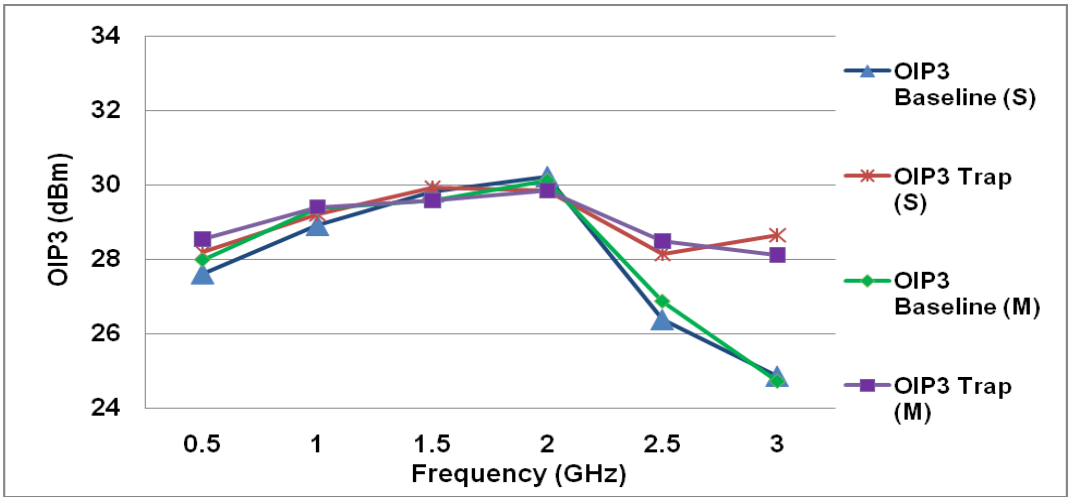

Figure 4.14: Simulated and measured OIP3 results for DA2

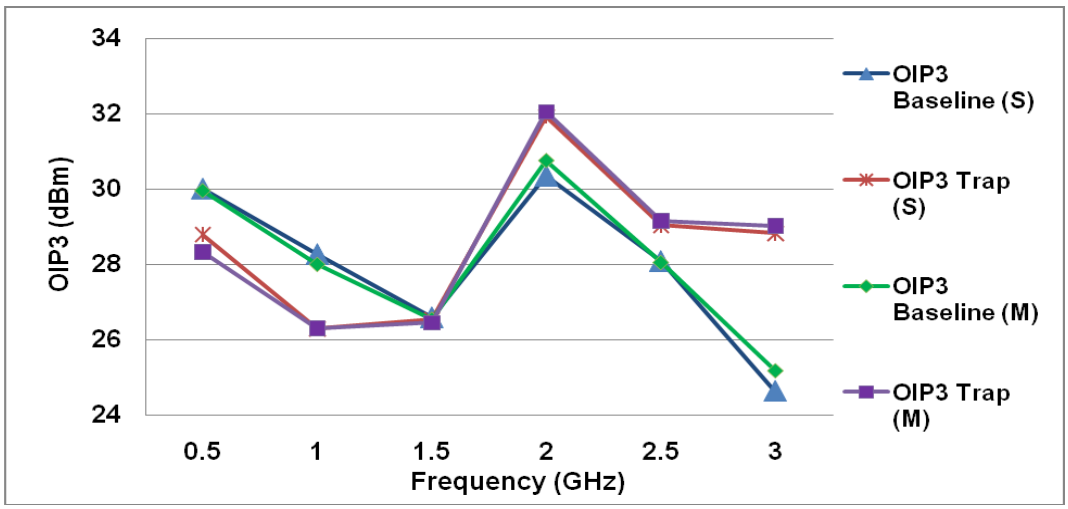

Figure 4.15: Simulated and measured OIP3 results for DA3

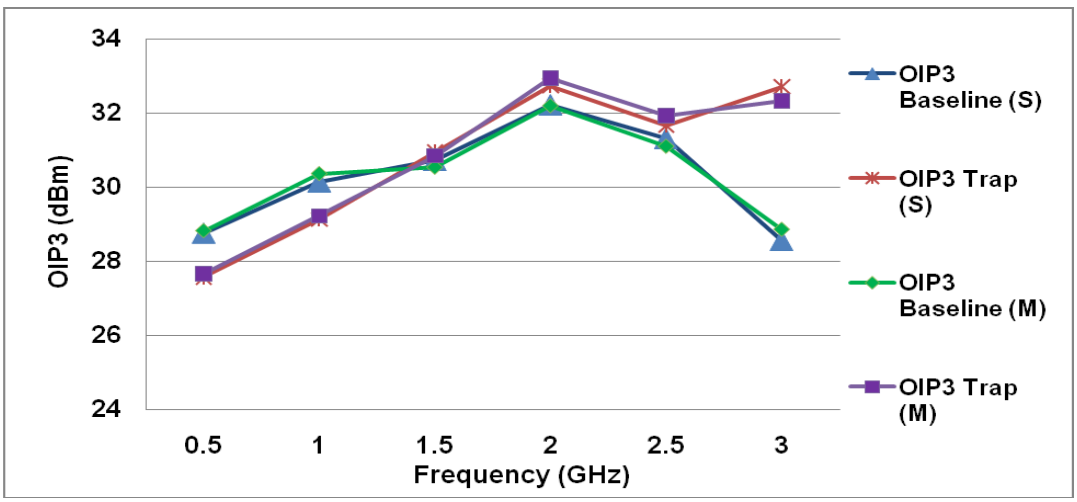

Figure 4.16: Simulated and measured OIP3 results for DA4

At 2.5 GHz and 3 GHz, the OIP3 is improved by 1.3 dB and 3.3 dB for DA1, 1.6 dB and 3.4 dB for DA2, 1.1 dB and 3.9 dB for DA3 and 0.8 dB and 3.5 dB for DA4. At lower frequencies, the improvement is negligible and there isn't much change in the linearity. The results concur with the fact that g_m nonlinearities become smaller at higher frequencies [127]. Placing the trap at the output of the HBT only causes a reduction of third order current in C_{bc}. It does not affect other nonlinearities which are dependent on g_m such as the voltage controlled current source, VCCS ($g_m V_{be}$), r_π (β/g_m) and C_{diff} ($g_m \tau$). So improvement can only be significant when the g_m nonlinearites start to decrease.

4.2.3.2 Varying Trap Capacitance

The inductor value used for the LC trap is changed to either 2.4 nH or 2.7 nH and the OIP3 is measured. Changing the inductor requires removing and soldering new SMT components onto the testboard. It is not possible to use inductor values such as a 2.5 nH inductor because they are not available in the market. Results from Figs. 4.17 to 4.20 indicate that the optimum component values for the LC trap are the 2.2 nF capacitor and 100 nH inductor since they result in the most improvement in OIP3.

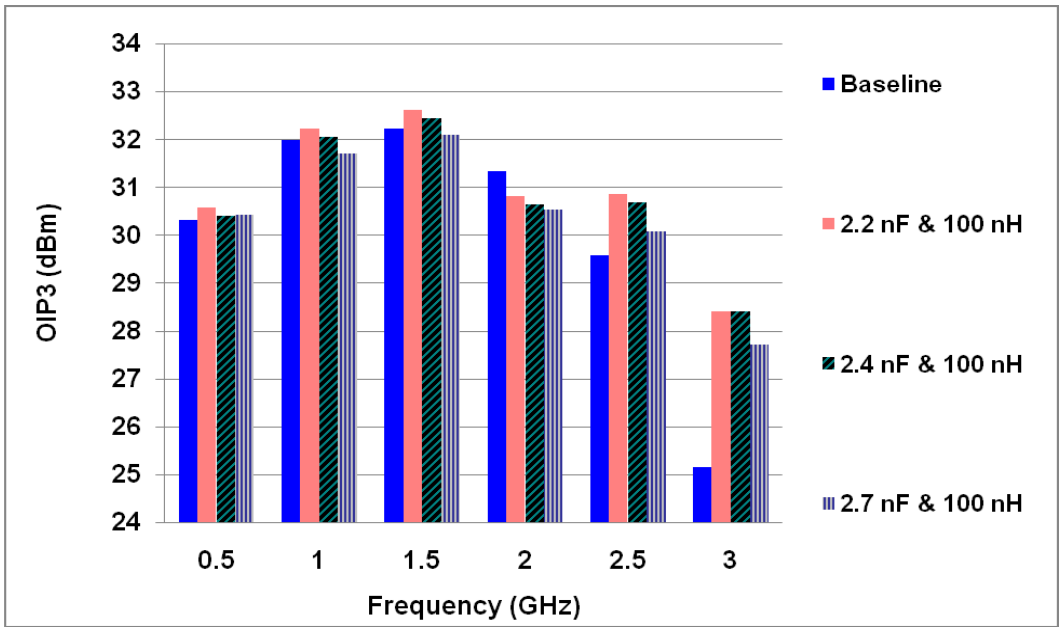

Figure 4.17: Measured OIP3 for DA1 with varying capacitance

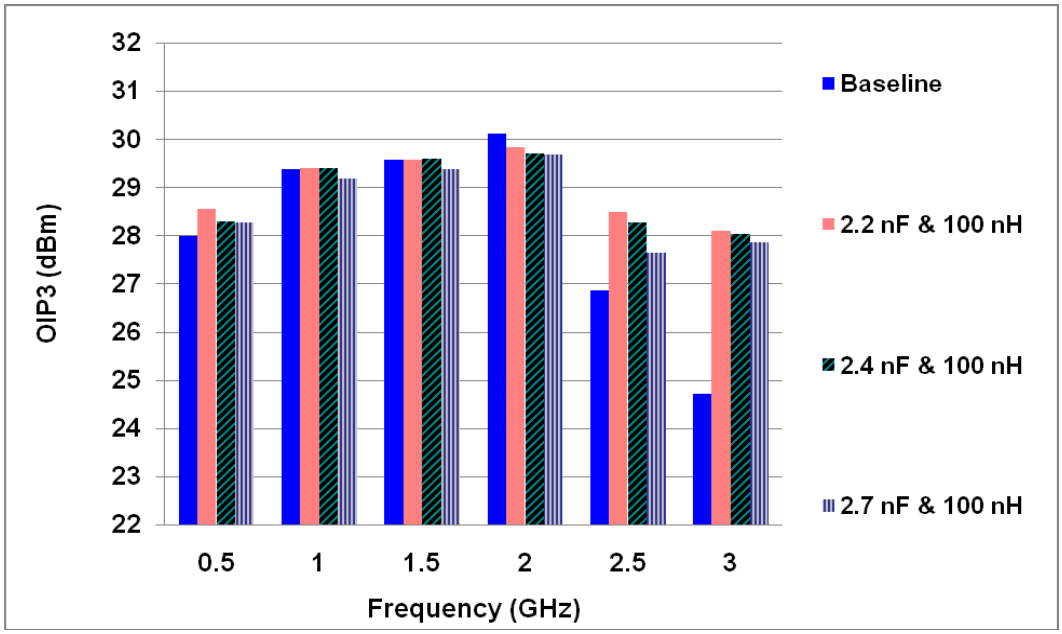

Figure 4.18: Measured OIP3 for DA2 with varying capacitance

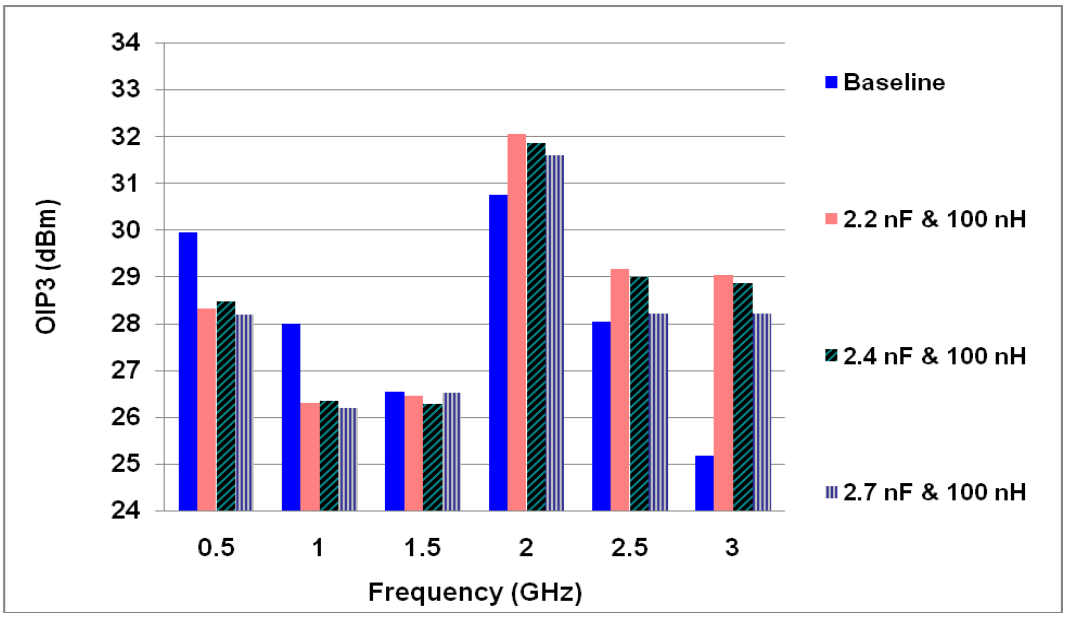

Figure 4.19: Measured OIP3 for DA3 with varying capacitance

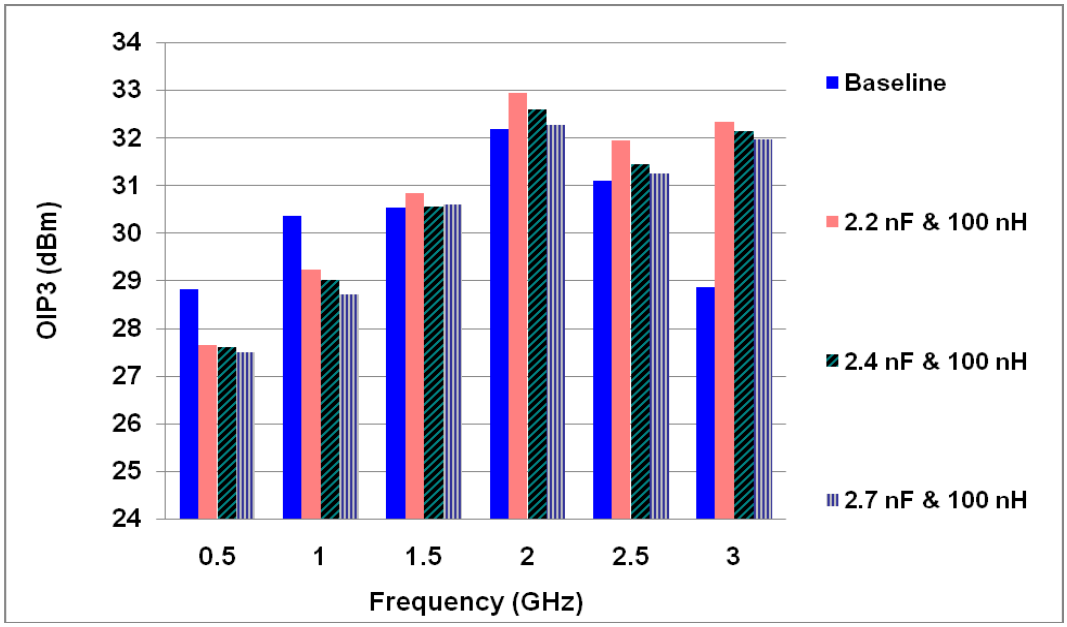

Figure 4.20: Measured OIP3 for DA4 with varying capacitance

4.3 Results from Implementing LC trap at Input of HBT

The first design iteration DAs are modified to include bond pads that bypass the C_{equ} and enable the LC trap to be placed directly at the base (input) of the HBT. This section contains results from measurements of the second design iteration DAs which are DA1A, DA1B and DA4A. Refer to Section 3.5.4 for the location of the LC trap at the input. In the following subsections, the results shown are with the LC trap values of 2.2 nF and 100 nH, unless specified otherwise. The base bias voltage, V_{be} is 1.375 V and the collector bias voltage, V_{ce} is 5 V (except in Section 4.3.3.5 where the base bias voltage is varied). The results in this section have been accepted for publication at the European Microwave Conference (EuMC) in Paris [15].

4.3.1 S-parameter Results

The simulated and measured S-parameter results are shown from Figs. 4.21 to 4.29 for DA1A, DA1B and DA4A. The second design iteration DAs were also tuned to have better input and output return losses. The S_{11} and S_{22} for all the designs are maintained at 10 dB or better, indicating a good input and output impedance match.

As mentioned in Section 4.2.1, the baseline measurements refer to the measurements done without the LC trap whereas measurements with the LC trap added to the circuit are referred to as “with trap”. S-parameter measurements that are the very close are measurements with and without the LC trap. The purpose of doing both these measurements is to show that the traps can help increase linearity without affecting the S-parameters. Again, different variants show the consistency of the conclusion that the LC traps do not affect the in-band gain and return loss.

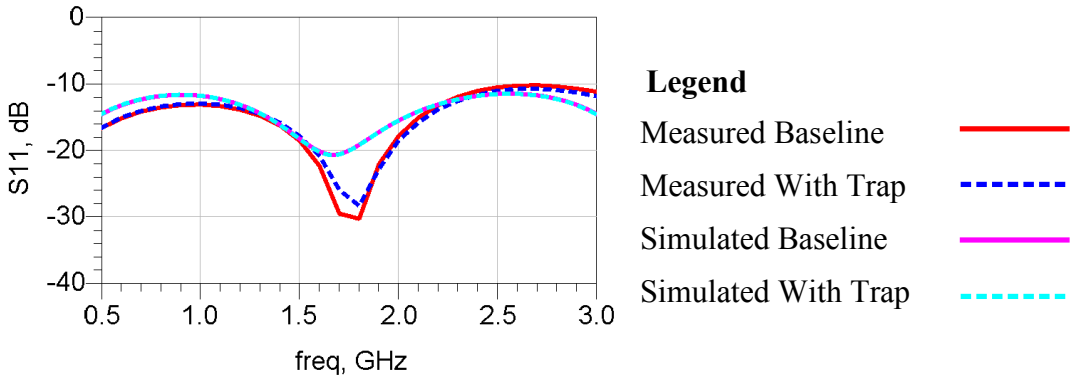

Figure 4.21: S_{11} results for DA1A with and without LC trap

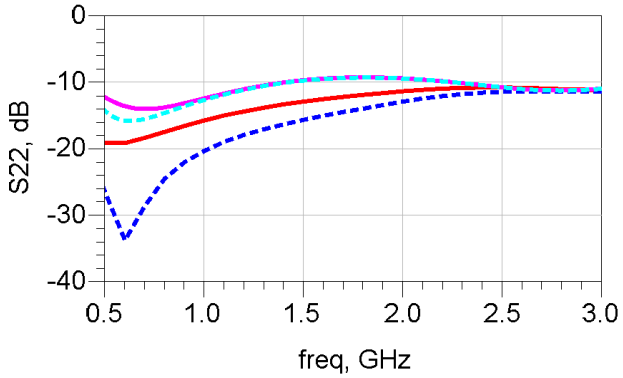

Figure 4.22: S_{22} results for DA1A with and without LC trap

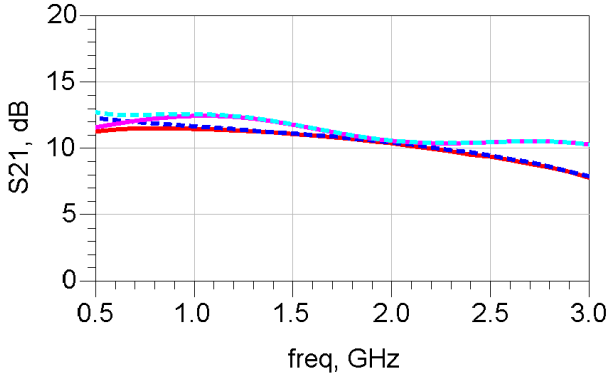

Figure 4.23: S_{21} results for DA1A with and without LC trap

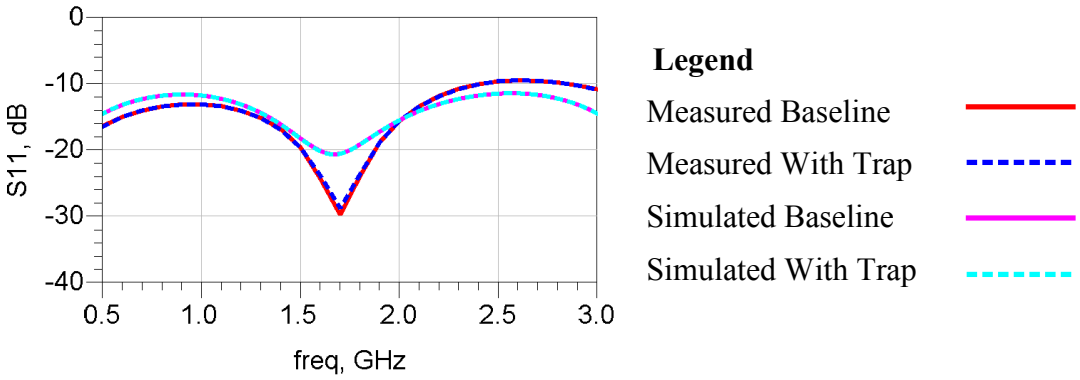

Figure 4.24: S_{11} results for DA1B with and without LC trap

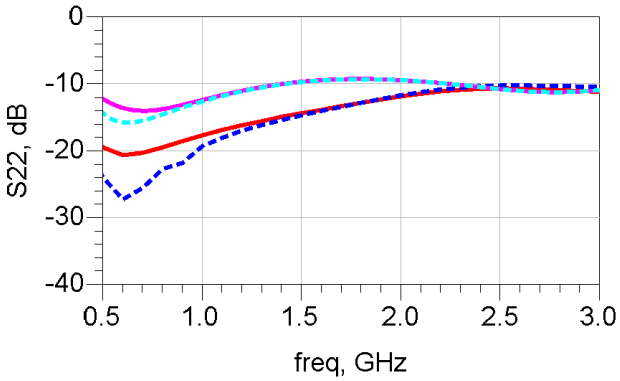

Figure 4.25: S_{22} results for DA1B with and without LC trap

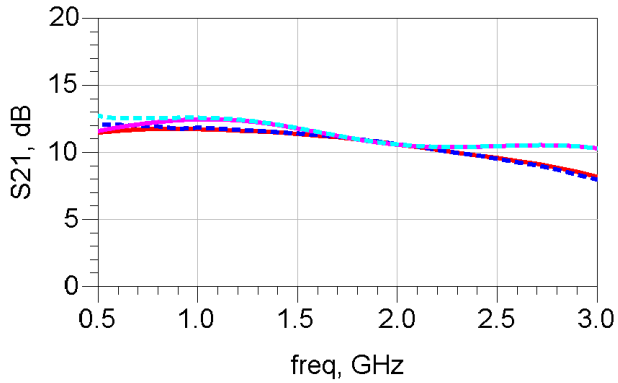

Figure 4.26: S_{21} results for DA1B with and without LC trap

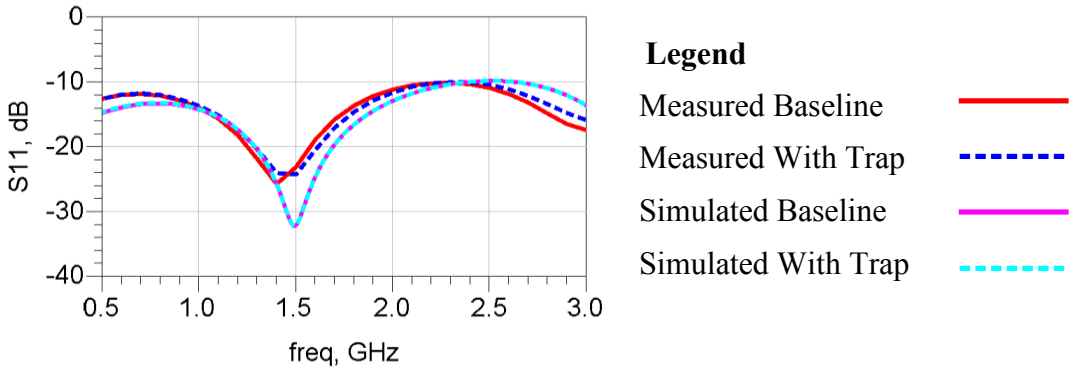

Figure 4.27: S_{11} results for DA4A with and without LC trap

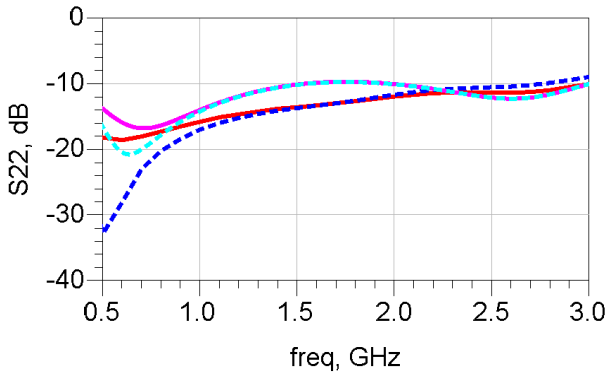

Figure 4.28: S_{22} results for DA4A with and without LC trap

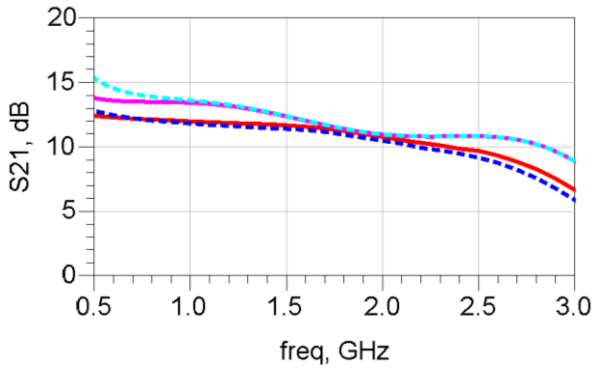

Figure 4.29: S_{21} results for DA4A with and without LC trap

The S_{21} or gain is maintained at +/- 1.5 dB throughout the band of operation, which is 0.5 GHz to 2.5 GHz. DA1A, DA1B and DA4A have an average measured gain of 10.3 dB, 10.5 dB and 11 dB, respectively. From the Figures, the measurement and simulated results concur with one another and the addition of the LC traps do not lower the in-band return loss and gain. This condition is desirable because linearity

can be increased by allowing S_{22} drops below 10 dB but this causes the device to fail the return los specifications.

4.3.2 P_{1dB} Results

The P_{1dB} is measured for 0.5 GHz to 3.0 GHz and at three separate base bias voltages and the results are in Table 4.3 to 4.5. From the data, it is shown that the addition of the traps does not affect the value of $P_{1dB.}$ The simulated results are close to the measured values with a maximum difference of less than 1 dB.

Increasing the base bias voltage generally results in more collector current and higher P_{1dB}, agreeing with the results shown in Section 4.3.2. The results in the Table 4.7 to 4.9 are tabulated from the P_{in} versus P_{out} data. This process is explained earlier in Section 3.13.2, where the measured baseline P_{1dB} for DA1B at 2.5 GHz (1.375 V) is 20.02 dBm.

Table 4.3: P_{1dB} for DA1A with and without LC trap

Type / Frequency	P_{1dB} at 0.5 GHz (dBm)	P_{1dB} at 1.0 GHz (dBm)	P_{1dB} at 1.5 GHz (dBm)	P_{1dB} at 2.0 GHz (dBm)	P_{1dB} at 2.5 GHz (dBm)	P_{1dB} at 3.0 GHz (dBm)
Base_1.35 V (S)	18.04	18.77	20.98	21.02	19.71	19.43
Base_1.35 V (M)	18.95	19.62	21.82	20.93	19.48	19.77
Trap_1.35 V (S)	19.83	18.88	21.03	20.99	18.85	19.32
Trap_1.35 V (M)	20.29	19.85	21.63	20.7	18.52	19.7
Base_1.375 V (S)	19.3	19.95	21.75	21.42	20.53	20.45
Base_1.375 V (M)	19.47	20.75	21.88	21.07	20.02	20.09
Trap_1.375 V (S)	20.01	20.05	21.76	21.44	20.72	20.25
Trap_1.375 V (M)	20.4	20.76	21.78	20.98	19.59	20.11
Base_1.4 V (S)	20.35	20.89	22.2	21.74	21.16	21.25
Base_1.4 V (M)	20.54	21.41	22.01	21.28	20.7	20.48
Trap_1.4 V (S)	20.91	20.94	22.22	21.72	21.37	20.96
Trap_1.4 V (M)	21.08	21.48	22.04	21.28	20.68	20.47

Table 4.4: P_{1dB} for DA1B with and without LC trap

Type / Frequency	P_{1dB} at 0.5 GHz (dBm)	P_{1dB} at 1.0 GHz (dBm)	P_{1dB} at 1.5 GHz (dBm)	P_{1dB} at 2.0 GHz (dBm)	P_{1dB} at 2.5 GHz (dBm)	P_{1dB} at 3.0 GHz (dBm)
Base_1.35 V (S)	18	18.73	21.04	21.06	19.68	19.41
Base_1.35 V (M)	18.95	19.49	21.78	21.09	19.37	20.25
Trap_1.35 V (S)	18.83	18.84	20.99	21.03	19.82	19.3
Trap_1.35 V (M)	19.61	19.5	21.7	20.78	19.13	20.04
Base_1.375 V (S)	19.3	19.96	21.76	21.41	19.92	20.42
Base_1.375 V (M)	19.66	20.62	21.9	21.06	20.02	20.26
Trap_1.375 V (S)	20.02	20.01	21.76	21.43	20.64	20.32
Trap_1.375 V (M)	20.11	20.63	21.87	21.06	20.07	20.23
Base_1.4 V (S)	20.35	20.85	22.21	21.69	21.17	21.22
Base_1.4 V (M)	20.67	21.36	22.05	21.29	20.83	20.52
Trap_1.4 V (S)	20.91	20.9	22.22	21.71	21.28	21.08
Trap_1.4 V (M)	20.93	21.32	22.02	21.3	20.91	20.47

Table 4.5: P_{1dB} for DA4A with and without LC trap

Type / Frequency	P_{1dB} at 0.5 GHz (dBm)	P_{1dB} at 1.0 GHz (dBm)	P_{1dB} at 1.5 GHz (dBm)	P_{1dB} at 2.0 GHz (dBm)	P_{1dB} at 2.5 GHz (dBm)	P_{1dB} at 3.0 GHz (dBm)
Base_1.35 V (S)	16.96	17.69	21.59	20.97	17.47	18.16
Base_1.35 V (M)	16.74	17.44	21.71	20.37	17.25	18.56
Trap_1.35 V (S)	17.95	17.86	21.68	20.95	17.35	18.16
Trap_1.35 V (M)	17.8	18.1	21.35	20.12	17.25	18.45
Base_1.375 V (S)	17.36	20.34	21.67	20.06	20.3	18.47
Base_1.375 V (M)	17.92	20.24	21.86	20.31	20.69	19.08
Trap_1.375 V (S)	18.25	19.25	21.72	20.01	20.29	18.39
Trap_1.375 V (M)	18.8	19.61	21.55	20.34	20.42	18.41
Base_1.4 V (S)	18.55	20.24	21.43	20.87	20.95	19.51
Base_1.4 V (M)	18.85	20.25	21.99	20.32	20.59	19.46
Trap_1.4 V (S)	19.37	20.35	21.49	20.88	21.05	19.34
Trap_1.4 V (M)	19.54	20.45	21.75	20.44	20.89	19.19

Table 4.6 shows the PAE at 2 GHz for DA1A to DA1B at P_{1dB}. The PAE is less than 25 % since the amplifier is biased at Class A and adding the traps does not cause a significant effect to the PAE.

Table 4.6: Power Added Efficiency at 2 GHz at P_{1dB} (Second design iteration DA)

Type	DA1A (%)	DA1B (%)	DA4A (%)
Baseline 1.35 V	23.62	24.34	23.78
Trap 1.35 V	22.21	22.58	22.4
Baseline 1.375 V	22.89	22.70	22.16
Trap 1.375 V	22.25	22.60	22.26
Baseline 1.4 V	22.38	22.31	21.01
Trap 1.4 V	22.21	22.27	21.56

4.3.3 OIP3 (Linearity) Results

The principle motivation behind this thesis is to increase the linearity (indicated by OIP3) of the DAs over a broadband. In this section, it will be shown that the addition of the LC traps at the input of the HBT fulfils this requirement. The improvement in linearity is examined using various capacitance and inductance values for the traps, differing base bias voltage and with varying the $f_{spacing}$ of the two tones.

4.3.3.1 P_{1dB} versus OIP3

The third order current, $I_{o,3}$ from Equation (3.46) was shown to depend on the source impedance at the envelope frequency, $Z_{s,2\omega 2-\omega 2}$. By presenting a low impedance termination, the linearity of the DA can be increased. Figs. 4.30 to 4.32 show that the traps have very minimal effect on P_{1dB}. Subsequently, the OIP3 for the DAs are improved throughout the frequency band with an average improvement of 5.3 dB for DA1A, 5.2 dB for DA1B and 3.28 dB for DA4A.

Improvement in OIP3 can be misleading if the OIP3 value above the P_{1dB} (OIP3-P_{1dB}) is not considered. The rule of thumb is for OIP3 to be 10 dB higher than

P_{1dB}. This is shown by the black dotted line in Fig. 4.30 to 4.32. The DAs without the trap, failed to achieve this mark at certain frequencies. With the addition of the traps, the OIP3 values have been increased above this level.

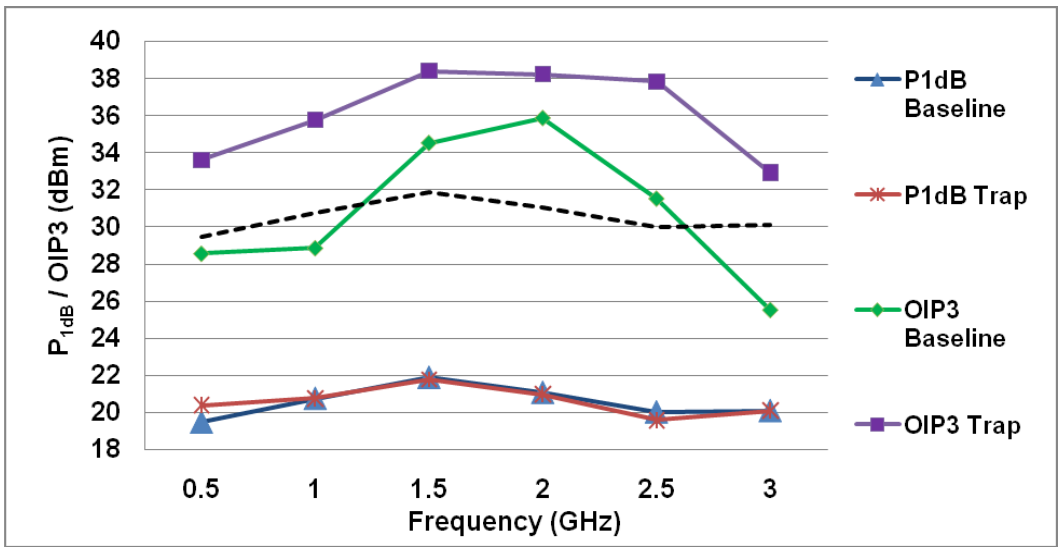

Figure 4.30: Measured P_{1dB} and OIP3 for DA1A with and without LC traps

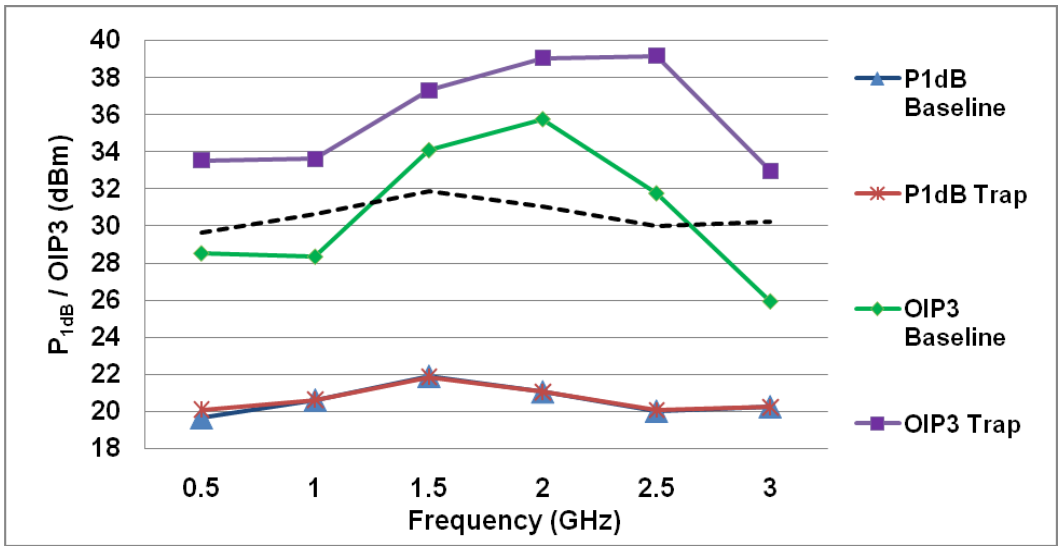

Figure 4.31: Measured P_{1dB} and OIP3 for DA1B with and without LC traps

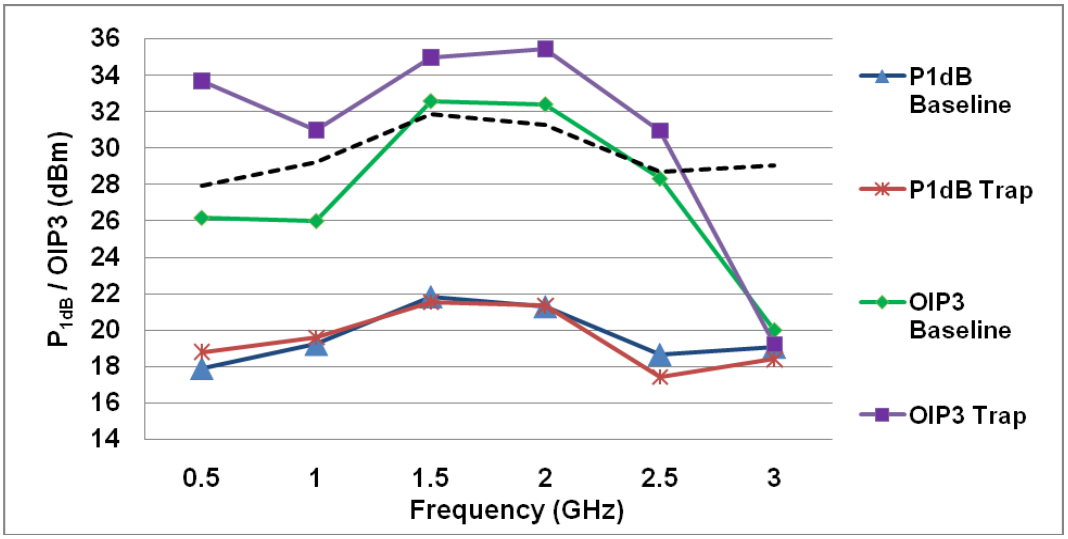

Figure 4.32: Measured P_{1dB} and OIP3 for DA4A with and without LC traps

From Fig. 4.30, at 0.5 GHz and 1.0 GHz, the OIP3 for DA1A is improved to 14.1 dB and 15 dB higher than P_{1dB}. At 2.5 GHz, the OIP3 is 17.82 dB above P_{1dB}. As shown in Fig. 4.31, the OIP3 for DA1B is improved by 13.9 dB and 13 dB higher than P_{1dB} at 0.5 GHz and 1.0 GHz. At 2.5 GHz, the OIP3 is 19.2 dB above P_{1dB}.

The OIP3 for DA4A is 15.8 dB and 11.7 dB above P_{1dB} at 0.5 GHz and 1 GHz respectively. At 2.5 GHz, the OIP3 is 12.3 dB above P_{1dB}. For DA4A (series ballasting DA), no improvement comes from using the LC trap at 3 GHz due to its faster gain roll-off compared to the DAs with parallel ballasting. The DAs have actually been designed to operate from 0.5 to 2.5 GHz.

4.3.3.2 Simulated versus Measured OIP3

Figs. 4.33 to 4.35 show the simulated and measured OIP3 for the DA1A, DA1B and DA4A. The simulated data are obtained by taking into account the testboard effects using Sonnet™ and by using the SMT models from Modelithics™. The trends between the simulated and measured results track well.

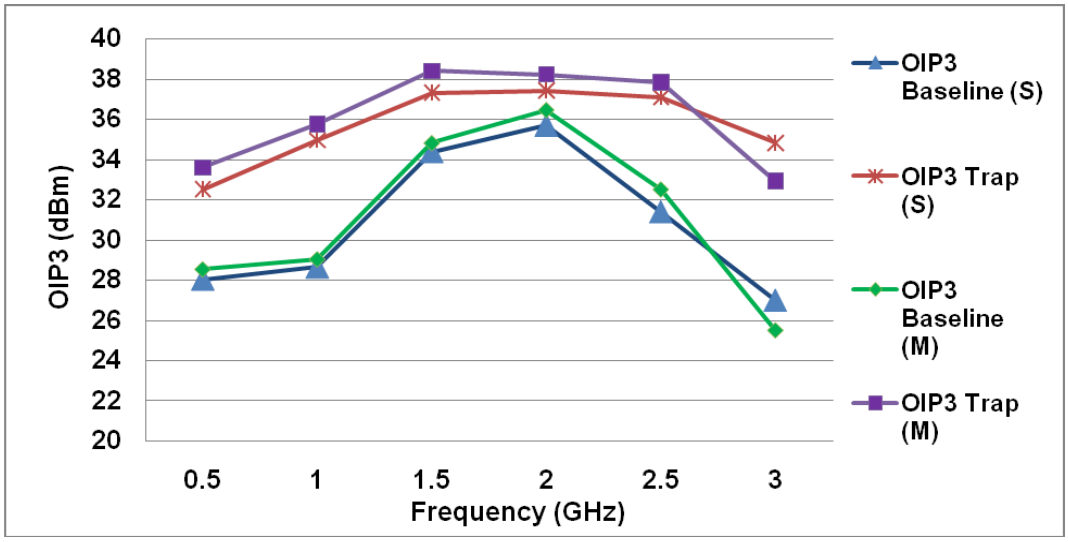

Figure 4.33: Simulated and measured OIP3 results for DA1A

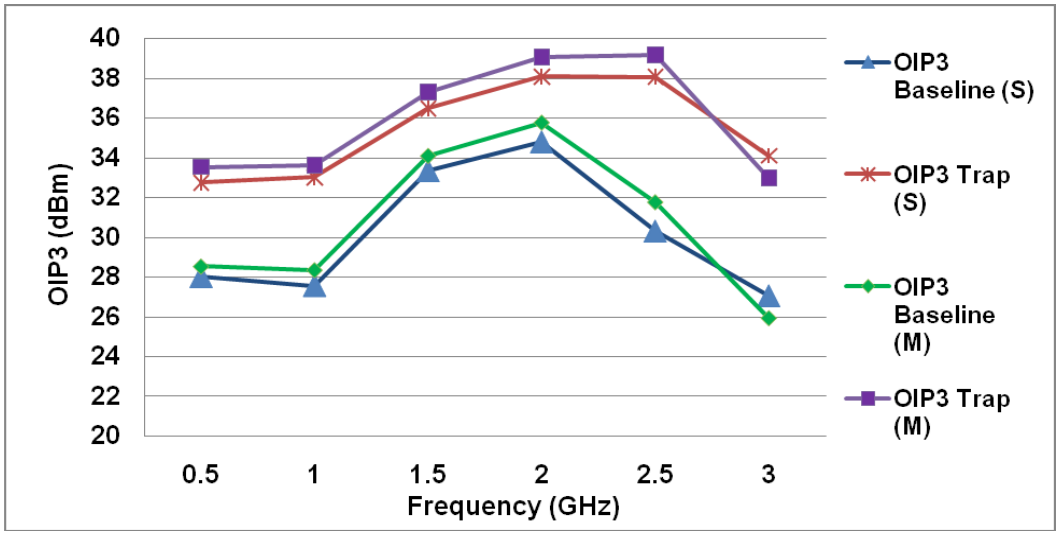

Figure 4.34: Simulated and measured OIP3 results for DA1B

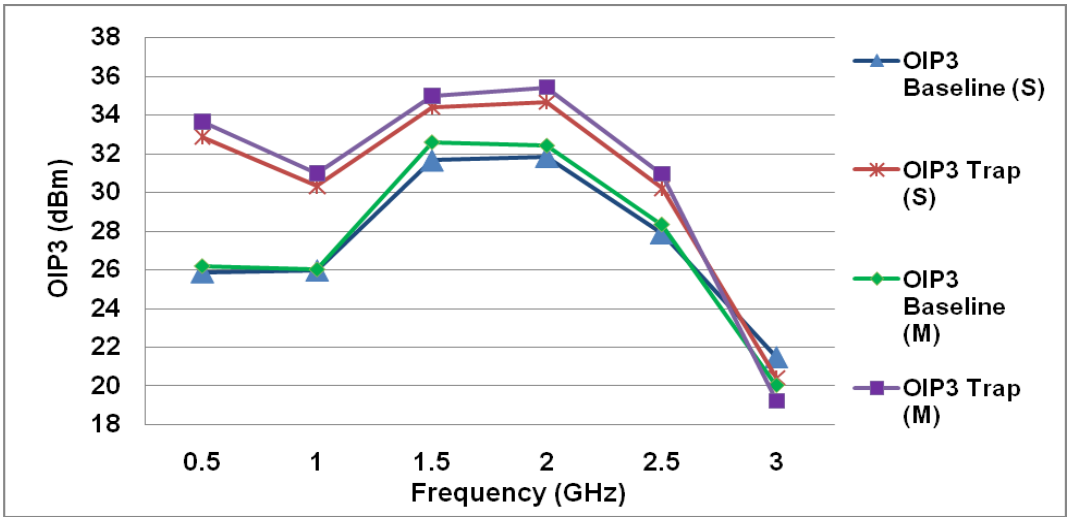

Figure 4.35: Simulated and measured OIP3 results for DA4A

4.3.3.3 Varying Trap Capacitance

To identify the optimum trap values for the LC trap, the capacitance value used in the trap is varied from 1 nF to 4.7 nF. The SMT components used are purchased from Murata. From Figs. 4.36 to 4.38, it is shown that the best improvement comes from using the 100 nH and 2.2 nF trap. With this trap values, the OIP3 for DA1A is improved from 2.4 dB to 7.4 dB, depending on frequency. For DA1B, the improvement ranges from 3.3 dB to 7.4 dB whereas for DA4A, the OIP3 is increased from 2.4 dB to 7.4 dB.

These results concur with the simulation results in Fig. 3.57 (Section 3.11.2) where the optimum impedance is nearly a short circuit with a small capacitive reactance and the maximum simulated improvement of 7.5 dB. This concurs with [111] that states the optimum termination is not zero but a complex value. The simulation is performed with a base bias voltage of 1.375 V. As the capacitance value of the trap is increased, the reactance of the trap becomes more inductive at the envelope frequency (10 MHz).

Reactance is the sum of the capacitive and inductive reactance

$$X_{total} = X_C + X_L = \frac{1}{2\pi fC} + 2\pi fL \tag{4.2}$$

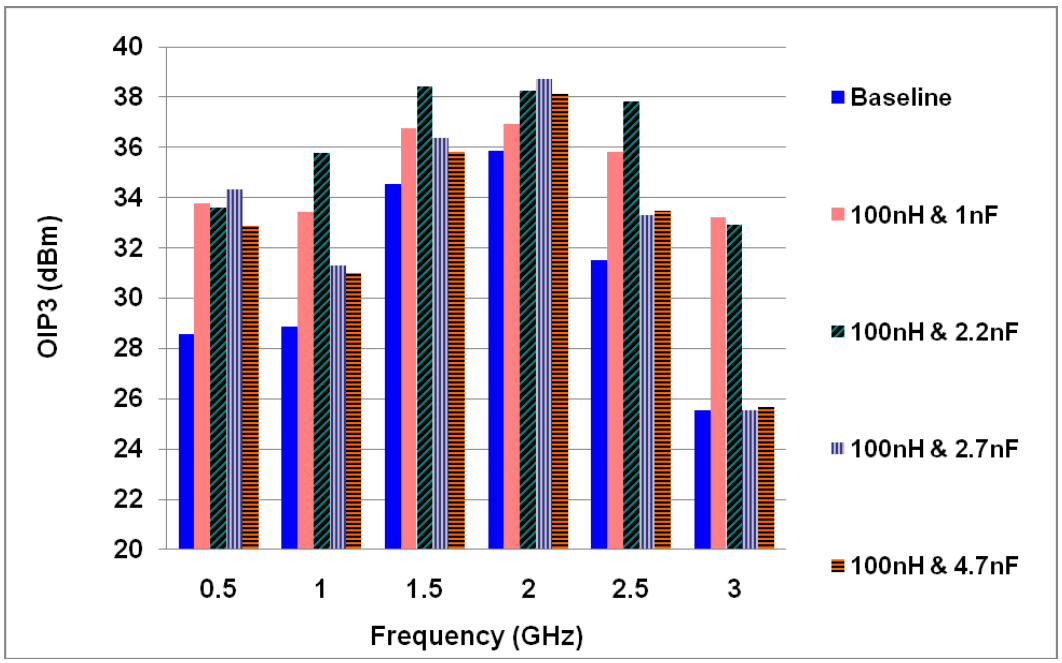

Figure 4.36: Measured OIP3 for DA1A with varying capacitance

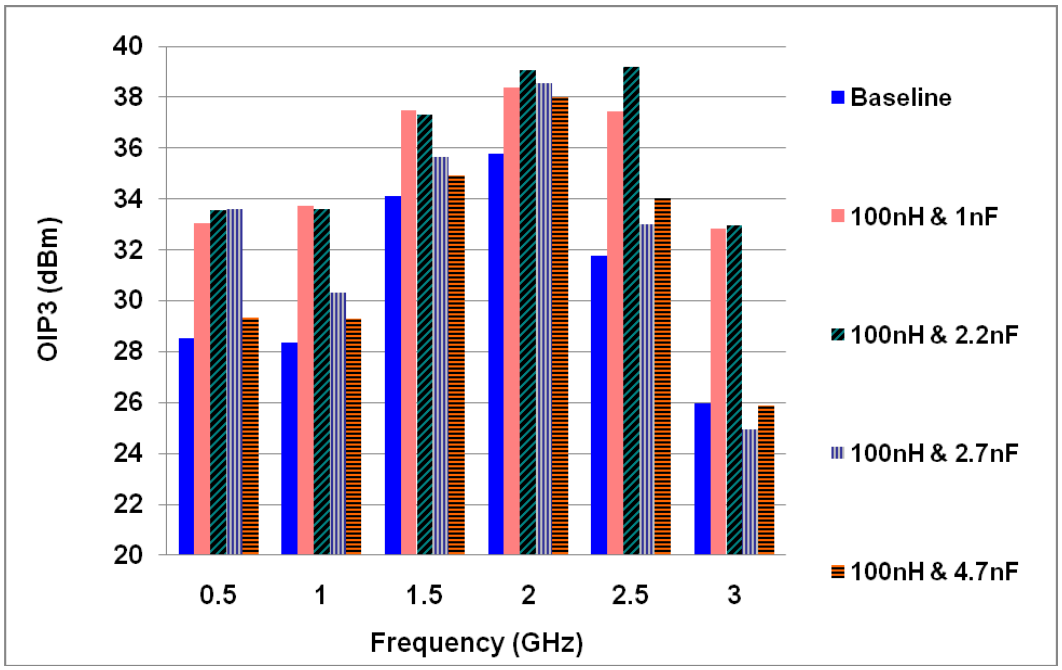

Figure 4.37: Measured OIP3 for DA1B with varying capacitance

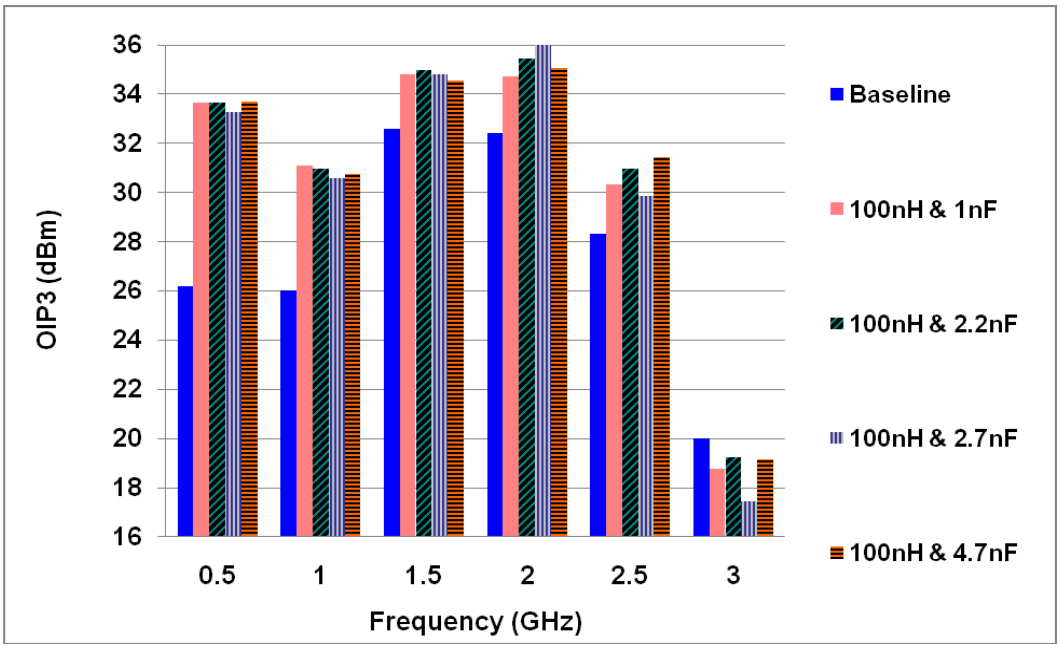

Figure 4.38: Measured OIP3 for DA4A with varying capacitance

4.3.3.4 Varying Trap Inductance

Since the increments in the values for commercially available SMTs for large inductors are quite big, it can be difficult to optimize the inductance values compared to the capacitance values for the trap. A large inductor must be used for the trap to avoid altering the in-band performance of the DA. When the inductor of the trap is varied, the 82 nH and 2.7 nF trap gives the best overall improvement in OIP3 for DA1A and DA4A. This improvement is varied from 1.8 dB to 5.5 dB for DA1A and 1.9 dB to 7.4 dB for DA4A. When varying the inductance of the trap for DA1B, the 100 nH and 2.7 nF trap gives the most improvement, ranging from 1.25 dB to 5 dB.

DA1B differs from DA1A and DA4A in the location of the LC trap. The trap for DA1B has an additional resistor, R_{sta} at each unit cell (Refer Fig. 3.27 in Section 3.5.1) as compared to DA1A and DA4A. The presence of resistance makes the trap response more selective. This is proven by comparing the results in Fig. 4.39 and 4.41 with Fig. 4.40.

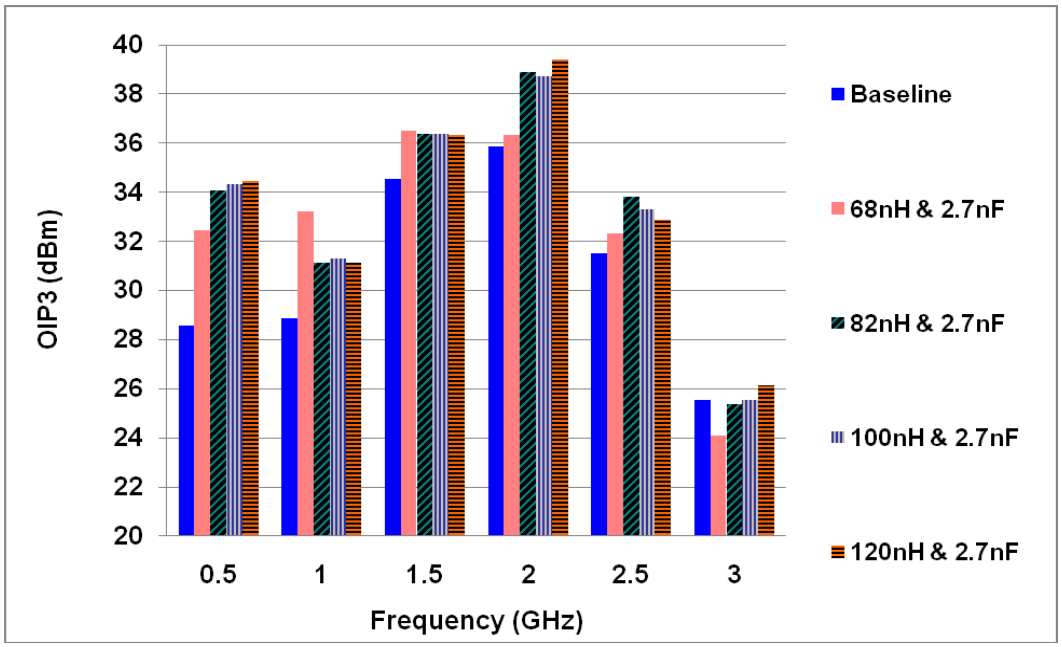

Figure 4.39: Measured OIP3 for DA1A with varying inductance

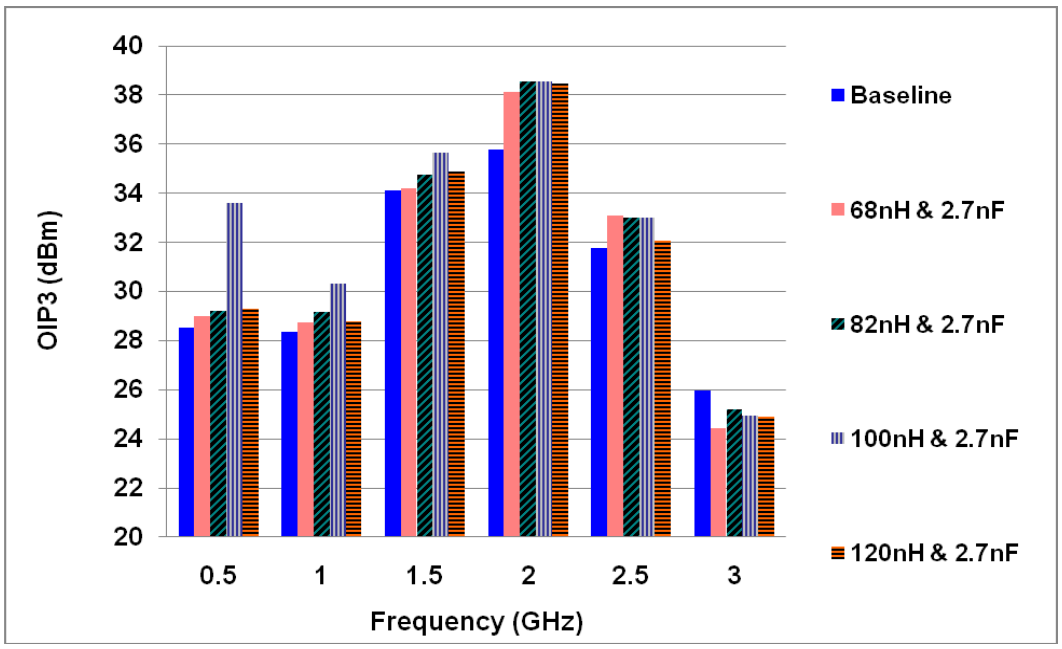

Figure 4.40: Measured OIP3 for DA1B with varying inductance

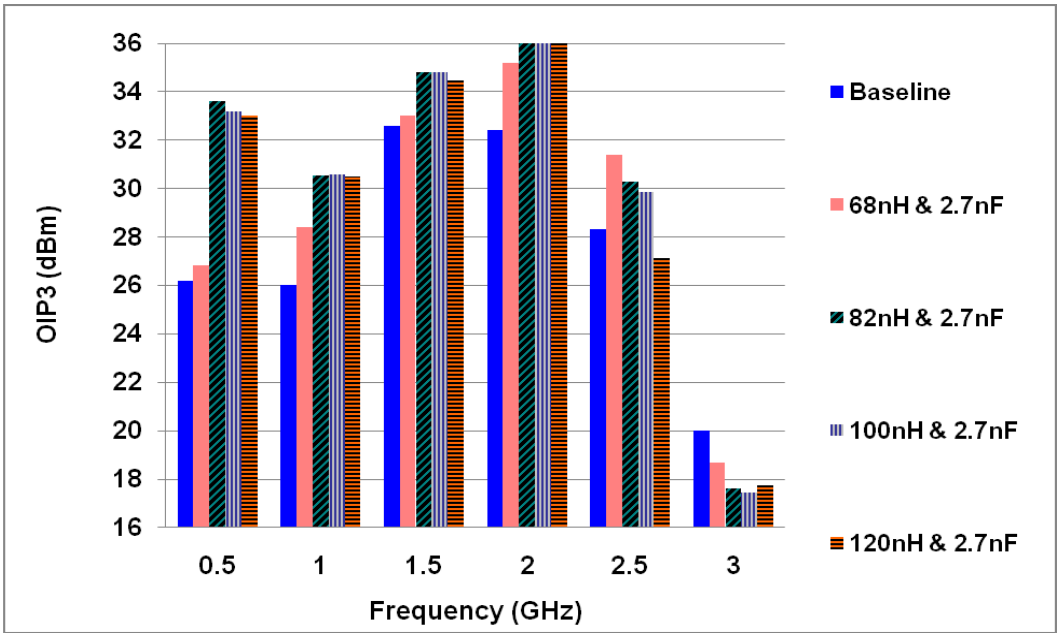

Figure 4.41: Measured OIP3 for DA4A with varying inductance

4.3.3.5 Varying Base Bias Voltage

Without the traps, larger base bias voltage (higher current operation) usually results in higher OIP3. This is shown by comparing the baseline values for Fig. 4.42 to 4.44. However, DA1A and DA1B with the traps can operate at a lower current and still maintain the OIP3 above 33 dBm. This is because the OIP3 is higher when operating at 1.375 V compared to 1.4 V. The reduction in current consumption is favourable since it saves power utilization and has higher efficiency. The simulated and measured total collector current at the various base bias voltages are shown in Table 4.7.

For DA4A, the trend of higher current resulting in higher OIP3 still remains because it uses series ballasting in its design. Ballasting design will affect the linearity performance of the DA. This result concurs with [112] which show that an optimum bias condition exists for linearity. For DA1A and DA1B, the optimum base bias voltage is at 1.375 V whereas for DA4A, a base bias of 1.4 V provides better linearity.

Table 4.7: Simulated and measured total collector current with various base bias voltage

Type	DA1A (S)	DA1A (M)	DA1B (S)	DA1B (M)	DA4A (S)	DA4A (M)
Collector current @ 1.35 V base bias voltage (mA)	42.03	42	42.03	42	37.77	37
Collector current @ 1.375 V base bias voltage (mA)	62.29	61	62.29	61	52.21	53
Collector current @ 1.4 V base bias voltage (mA)	80.23	81	80.23	81	70.4	71

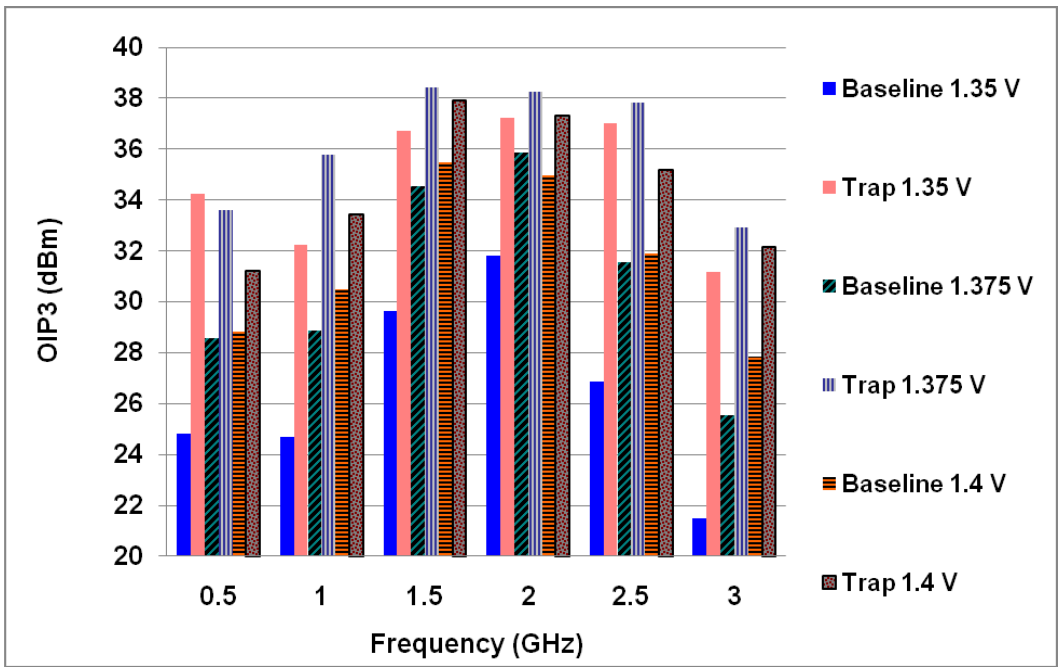

Figure 4.42: Measured OIP3 for DA1A with varying base bias voltage

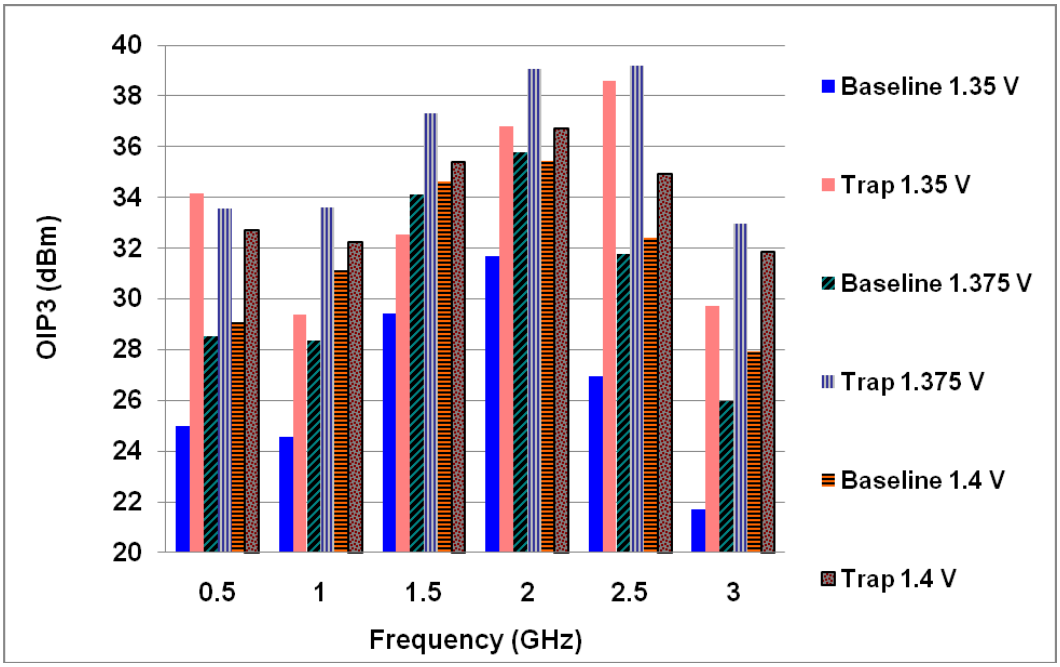

Figure 4.43: Measured OIP3 for DA1B with varying base bias voltage

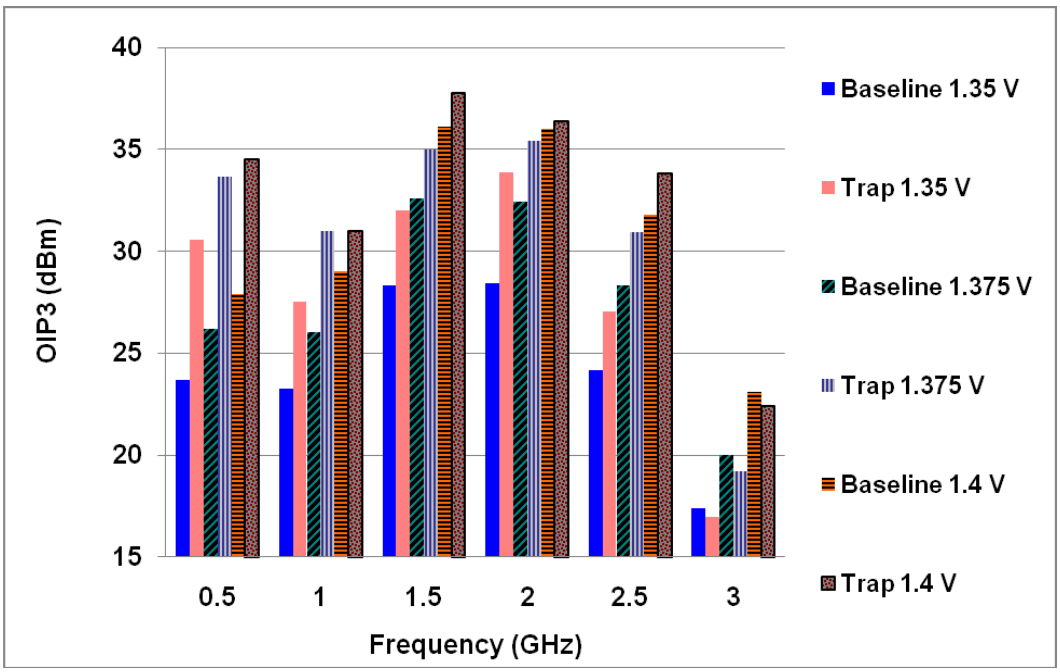

Figure 4.44: Measured OIP3 for DA4A with varying base bias voltage

Comparing the three figures above, the improvement in terms of OIP3 from the baseline is larger at lower base bias voltage. For example, for DA1B, at 2.5 GHz, the improvement is 11.6 dB at 1.35 V, 7.4 dB at 1.375 V and 2.52 dB for 1.4 V. Although

the improvement is larger at 1.35 V, the optimum bias is still at 1.375 V because generally the OIP3 (with the traps) is still higher at 1.375 V compared to at 1.35 V.

4.3.3.6 Varying fspacing (Δf)

Fig. 4.45 to 4.47 are the results for the linearity when the $f_{spacing}$ between the two tones are varied while maintaining the center frequency at either 1, 2 or 3 GHz. Improvement in OIP3 is still maintained and the variation in OIP3 is less than 7%. Nevertheless, the best improvement in linearity still occurs when the $f_{spacing}$ is the same as the trap resonant frequency. The $f_{spacing}$ in this project is also refered to as the envelope frequency (ω_2-ω_1). The trap resonant frequency is given by

$$f_R = \frac{1}{2\pi\sqrt{L_{trap}C_{trap}}} \tag{4.3}$$

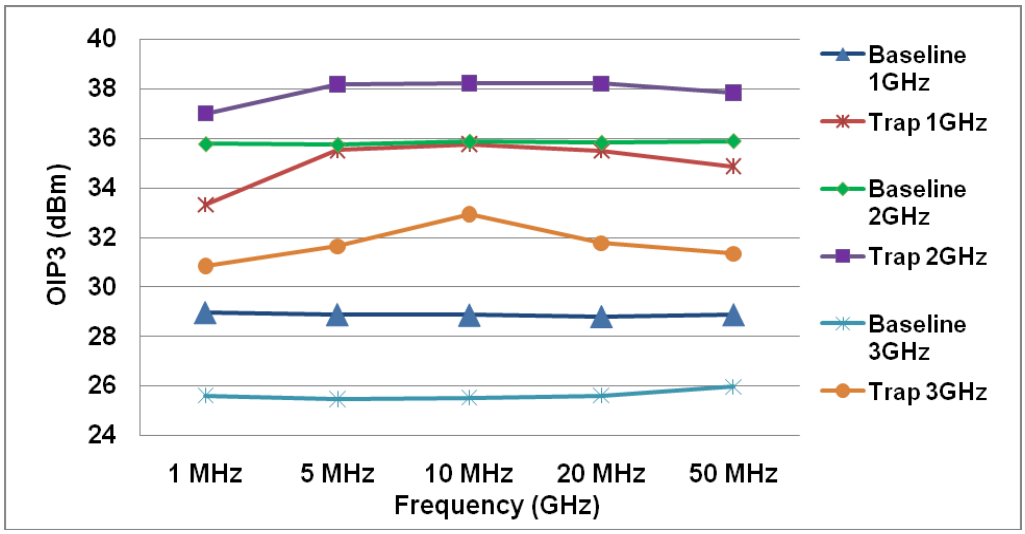

Figure 4.45: Measured OIP3 for DA1A with varying $f_{spacing}$

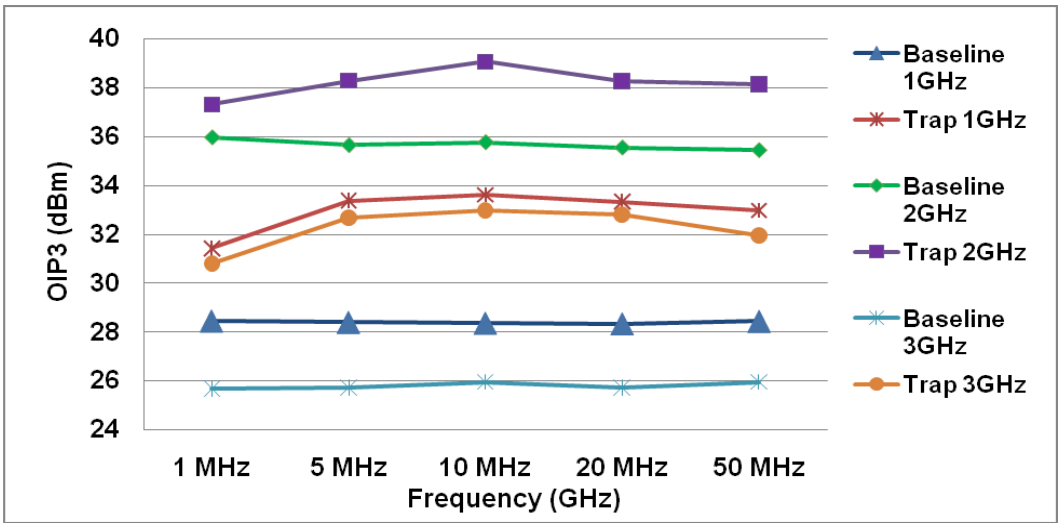

Figure 4.46: Measured OIP3 for DA1B with varying $f_{spacing}$

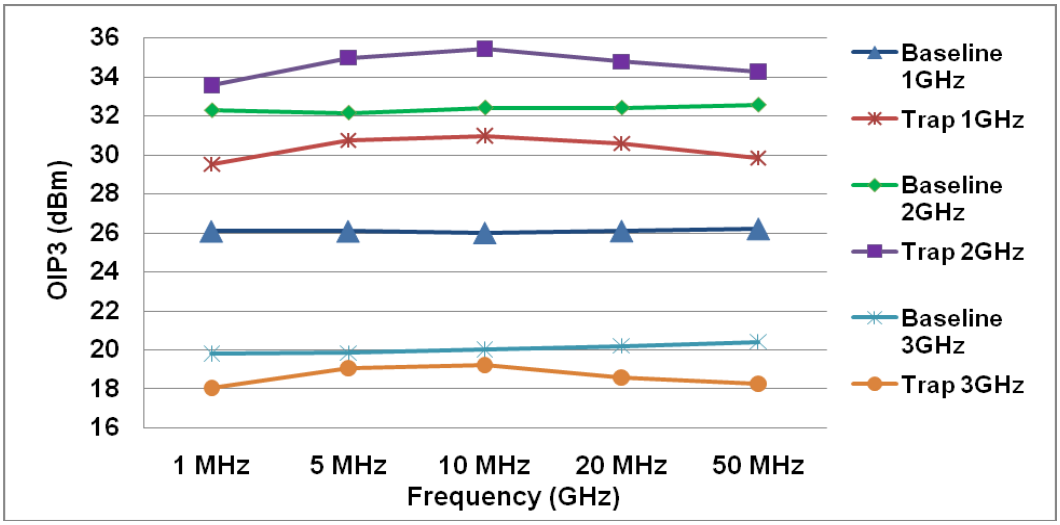

Figure 4.47: Measured OIP3 for DA4A with varying $f_{spacing}$

4.4 Comparison with Other Work Using Low Impedance Termination

Placing an optimum termination at either the source or load of the HBT has been accomplished in various device technologies to order to improve the linearity of a device in a narrowband [9]-[13], [111].

However, no reports have been made on the use of the terminations to improve broadband linearity, making it the novelty of this research. The linearity of the DA over a bandwidth of 0.5 to 3 GHz (6:1 bandwidth) is improved by a range of 2.4 dB to 7.4 dB for DA1A, 3.3 dB to 7.4 dB for DA1A and 2.4 to 7.4 dB for DA4A. Table 4.8 summarizes and provides a comparison of the linearization projects with the low impedance termination method. The work in this thesis is highlighted in bold. The improvement in linearity is higher for the work done by other researchers because the low impedance terminations are set to short out both the envelope and second harmonic frequencies. In this project, to ensure that the in-band performance of the DA is not affected, the terminations only provide low impedance at the envelope frequency.

Table 4.8: Comparison of research done using low impedance terminations

Technology	**Frequency (GHz)**	**Device Type**	**Improvement to linearity (dB)**	**Reference**
Philips QuBiC3 BiCMOS	0.9	LNA	8.35	[9]
Philips QuBiC3 BiCMOS	2	LNA	7.25	[9]
Si BJT	2	LNA	14	[10]
0.4 μm SiGe BiCMOS	1.96	LNA	9	[12]
Philips BFG11 BJT	1.8	LNA	8	[13]
2 μm InGaP/GaAs HBT	**0.5-3.0**	**DA**	**7.4**	**[15]**

4.5 Summary

This chapter includes all the results from measurements with the first and second design iterations of the DA. Measurements were performed with and without the traps to view its impact on the S-parameters, P_{1dB} and OIP3. Measurements without any traps added to the die are referred to as the baseline measurements. Simulations for the S-parameters, P_{1dB} and OIP3 track well with the measured values.

All the DA variants satisfy the requirements of having a minimum gain of 10 dB and a minimum P_{1dB} of 17 dBm (~50 mW). The input and output return losses are also maintained to be 10 dB or better. The average measured gain is 11.6 dB for DA1, 13.7 dB for DA2, 10.6 dB for DA3 and 12.5 dB for DA4. The P_{1dB} with the addition of the trap is 20.91 dB for DA1, 20.90 dB for DA2, 20.74 dB for DA3 and 20.70 dB for DA4 at 2 GHz. The average measured gain is 10.3 dB, 10.5 dB and 11 dB for DA1A, DA1B and DA4A, respectively. The P_{1dB} with the presence of the traps, at 2 GHz is 20.98 dB for DA1A, 21.06 dB for DA1B and 20.34 dB for DA4A.

After the addition of the LC trap at the output of the DA, improvement in linearity only occurs at the higher frequencies. At 2.5 GHz and 3 GHz, the OIP3 is improved by 1.3 dB and 3.3 dB for DA1, 1.6 dB and 3.4 dB for DA2, 1.1 dB and 3.9 dB for DA3 and 0.8 dB and 3.5 dB for DA4. The improvement is negligible at the lower frequencies since there isn't much change in the linearity.

Traps at the input of the HBT results in a linearity improvement throughout the band of 0.5 GHz to 3.0 GHz. At the optimum trap of 100nH and 2.2 nF, the improvement in OIP3 for DA1A is varies from 2.4 dB to 7.4 dB, depending on frequency. For DA1B, the improvement ranges from 3.3 dB to 7.4 dB and for DA4A, the OIP3 is increased from 2.4 dB to 7.4 dB. In addition, placing the traps at the input or output of the DA does not significantly lower the P_{1dB} or affect the in-band S-parameters.

CHAPTER 5
CONCLUSION

5.1 Introduction

The power amplifier is one of the most critical components in a transreceiver because its signal integrity influences the performance of the entire system. There are strict regulatory requirements on its linearity and must be increased since filters cannot fully remove the third order intermodulation products which are too close to the fundamental tones. These products, if too large, will cause distortion and affect the system's capability of differentiating between the intended signals and the third order harmonic products. These third order products exist since amplifiers are nonlinear systems. One characteristic of nonlinear systems is the generation of intermodulation products whenever two or more closely spaced signals enter the amplifier. It is difficult to maintain high output power and linearity at the same time without linearization techniques. These two values can be traded off for each other but is undesirable. This project has successfully implemented the LC trap method as a linearization technique over a broad band of 0.5 GHz to 3.0 GHz.

5.2 Conclusion

The future of the RF world is in the direction towards reconfigurable systems which can switch between different telecommunication standards such as CDMA, GSM and UMTS. However, having a reconfigurable system requires coming up with design architectures that are able to achieve high linearity over a broad bandwidth. This research takes a step in that direction by improving the linearity over a bandwidth of

0.5 GHz to 3.0 GHz (6:1 bandwidth ratio) for InGaP/GaAs HBT Distributed Amplifiers using low impedance terminations at the envelope frequencies either at the input or output of the DA. Here lies the novelty of this work since no other work has been made regarding improving broadband linearity using envelope terminations.

The reason the InGaP/GaAs HBTs device technology was chosen for this project because GaAs has better power handling compared to Si due to its higher breakdown voltage and larger maximum currents. Furthermore, GaAs has much higher minority carrier mobility compared to Si over a wide range of acceptor doping, making it suitable for designs that require high speed operations. GaAs also has the ability to form latticed-matched heterojunctions that cannot be achieved using traditional Si devices. HBTs have a wider bandgap material in the emitter (such as AlGaAs or InGaP), thereby increasing injection efficiency and current gain over regular bipolar transistors. HBTs also have higher power density compared to FETs. The InGaP is chosen as the emitter material for the HBT as opposed to AlGaAs since it has a larger valence band discontinuity resulting in a larger increase in the current gain.

Increasing linearity has always been a major concern for RF amplifier designers and is taken into consideration at the very beginning of the design process. The reason the distributed amplifier configuration is chosen is because it can easily achieve more than one octave in bandwidth, though the linearization method should be applicable to all amplifier types since it has been proven in this work that it is successful even for a broadband amplifier.

All the objectives for this project have been successfully completed. Two design iterations for the DA were made. Schematic design and layout of the DAs have been carried out using ADS. The first design iteration has four variants; DA1, DA2, DA3 and DA4 where DA1 and DA2 use parallel ballasting resistors and DA3 and DA4 use series ballasting resistors. The first design iteration was to test the effects of placing the low impedance termination (LC trap) at the collector line or output of the DA. The second design iteration has three variants; DA1A, DA1B and DA4A where DA1B and DA1B are modified versions of DA1 and DA4A is based on DA4. The second design iteration was to test the effects of placing the low impedance termination at the

base or input of the DA. DA1A and DA1B differ in the placement of the LC trap. DA1A has the LC trap after the stabilizing resistor, directly to the base of the HBT while for DA1B, the LC trap is placed before the stabilizing resistor.

The first and second design iterations were fabricated using the WIN H02U-41 and H02U-43 InGaP/GaAs HBT foundry process, respectively. This is a 2 μm HBT process with f_T = 31 GHz, f_{max} = 110 GHz, I_{DC} current gain = 75 and breakdown voltages BV_{CEO} = 17 V, BV_{BEO} = 7 V, BV_{CBO} = 30 V. The transistor used in these designs is the RQ1A202F2_M2 HBT. It has a two emitter fingers with the width and length of each emitter mesa are 2 μm and 20 μm respectively, giving an emitter periphery of 80 μm^2. The size of the first iteration DA MMIC die is 2020 μm by 660 μm while the size of the second iteration DA MMIC die is 1620 μm X 660 μm.

From measurements of the DAs, the requirement of having a minimum gain of 10 dB and a minimum P_{1dB} of 17 dBm (~50 mW) are satisfied. The input and output return losses are also maintained to be 10 dB or better. The average measured gain is 11.6 dB for DA1, 13.7 dB for DA2, 10.6 dB for DA3 and 12.5 dB for DA4. At 2 GHz, the P_{1dB} with the addition of the trap is 20.91 dB for DA1, 20.90 dB for DA2, 20.74 dB for DA3 and 20.70 dB for DA4. For the second design iteration, the average measured gain is 10.3 dB, 10.5 dB and 11 dB for DA1A, DA1B and DA4A, respectively. The P_{1dB} with the presence of the traps, at 2 GHz and a base bias voltage of 1.375 V is 20.98 dB for DA1A, 21.06 dB for DA1B and 20.34 dB for DA4A.

Two design iterations of the testboard were also made using AutoCAD and fabricated to accommodate external tuning elements and the LC traps. These testboards have a size of 40 mm by 50 mm and uses the Grounded CPW as a transmission media. The strip width and spacing for the ground planes were be selected to yield a characteristic impedance of 50 Ω.

The linearity improvement technique presents a low impedance termination at the envelope frequency to the input or output of the DAs to lower the generation of third order intermodulation currents. This termination, also known as an LC trap, is a series inductor-capacitor network implemented external to the MMIC die. To avoid interfering with the in-band performance of the DA, a large inductor (such as 100 nH)

must be used. This means that the trap must be implemented external to the MMIC die because it would be impractical to put such a large inductor onto the MMIC. Terminations at the second harmonic frequencies can also affect the linearity, but are disregarded since they provide a short circuit at the in-band frequencies.

Simulations for the small signal S-parameters and large signal parameters such as P_{1dB} and OIP3 track well with the measured values. The simulations were performed using ADS with WIN's VBIC large signal HBT model. Effects from the testboard are also taken into account by including results from electromagnetic simulations using the Sonnet™ software.

An analysis of the HBT nonlinear model shows that the third order intermodulation current generated by C_{bc}, a nonlinear component in HBTs, is dependent on the base-collector voltage at second order frequencies (such as ω_2-ω_1 and $2\omega_2$). The envelope frequency is at ω_2-ω_1 and placing the LC trap at the collector-emitter junction affects V_{bc} as well. By placing the LC trap at the output of the DA, improvement in linearity only occurs at the higher frequencies. At 2.5 GHz and 3 GHz, the OIP3 is improved by 1.3 dB and 3.3 dB for DA1, 1.6 dB and 3.4 dB for DA2, 1.1 dB and 3.9 dB for DA3 and 0.8 dB and 3.5 dB for DA4. The improvement is negligible at the lower frequencies since there isn't much change in the linearity.

These results concur with the fact that the g_m nonlinearity becomes smaller at higher frequencies. Placing the trap at the output of the HBT only causes a reduction of third order current in C_{bc}. It does not affect other nonlinearities which are dependent on g_m such as the voltage controlled current source, VCCS ($g_m V_{be}$), r_π (β/g_m) and C_{diff} ($g_m\tau$). The improvement can only be significant when the g_m nonlinearity begins to decrease. This improvement occurs without significantly lowering P_{1dB} or affecting the in-band S-parameters. This is desirable because linearity has been known to increase when S_{22} drops below 10 dB but this causes the device to fail the specifications for the return loss.

The analysis of the HBT model shows that the r_π, C_{be} and $g_m V_{be}$ nonlinearities are dependent on the base-emitter voltage at the envelope frequency, $V_{be,\omega 2-\omega 1}$, which in

turn can be altered by changing the impedance at the envelope frequency, $Z_{S,\omega 2-\omega 1}$. Simulations in MATLAB show that the optimum impedance is a short circuit with a small capacitive reactance and results in a 15 dB reduction in third order current. This means that the OIP3 can be increased by 7.5 dB which is close to the maximum measured improvement of 7.4 dB.

For the second DA design iteration, the inductor and capacitor values for the traps, base bias voltage and $f_{spacing}$ are varied. At the optimum trap of 100nH and 2.2 nF, the improvement in OIP3 for DA1A is varies from 2.4 dB to 7.4 dB, depending on frequency. For DA1B, the improvement ranges from 3.3 dB to 7.4 dB whereas for DA4A, the OIP3 is increased from 2.4 dB to 7.4 dB. At 2.5 GHz, the OIP3 for DA1A, DA1B and DA4A is 17.8 dB, 19.2 dB and 12.3 dB above P_{1dB} respectively.

Since the increments in the values for commercially available SMTs for large inductors are quite big, it is difficult to optimize the inductance values compared to the capacitance values for the trap. A large inductor must be used for the trap to avoid altering the in-band performance of the DA. DA1B differs from DA1A and DA4A in the location of the LC trap. The trap for DA1B sees an additional resistor, R_{sta} at each unit cell as compared to DA1A and DA4A. The presence of resistance makes the trap response more selective.

Without these traps, larger base bias voltage (higher current operation) is usually required for higher OIP3. However, DA1A and DA1B with the traps can operate at a lower current and still maintain the OIP3 above 33 dBm. This is because the OIP3 is higher when operating at 1.375 V compared to 1.4 V. The reduction in current consumption is favourable since it saves power utilization and has higher efficiency. For DA4A, the trend of higher current resulting in higher OIP3 still remains because it uses series ballasting in its design. An optimum bias condition exists for linearity and the ballasting design affects the bias condition. For DA1A and DA1B, the optimum base bias voltage is at 1.375 V whereas for DA4A, a base bias of 1.4 V provides better linearity.

Improvement in OIP3 is still achieved with variation of is less than 7% when the $f_{spacing}$ between the two tones is varied while maintaining the center frequency at either 1, 2 or 3 GHz. Nevertheless, the best improvement in linearity still occurs when the $f_{spacing}$ is the same as the trap resonant frequency of 10 MHz.

Placing the LC trap at the output only results in improvment OIP3 at the higher frequencies. Traps located at the input of the HBT can bring about improvement in OIP3 throughout the entire band of 0.5 GHz to 3.0 GHz since the other nonlinearities such as r_π, C_{be} and g_m depend on the source impedance at the envelope frequency. These improvements are significant because other in-band parameters such as gain, return loss and P_{1dB} are not lowered. This project has been successful in demonstrating a novel effort to improve broadband linearity with low impedance envelope terminations. Comparisons with other work show that this technique is mostly applied to LNAs and to narrowband applications.

5.3 Contributions Made

There are several important contributions from this project. Firstly, the LC trap method has been proven successful in improving the linearity over a broadband. In previous work, both the second harmonic and envelope frequencies were shorted out by the traps. However, this project modifies the method for broadband usage by tuning only the envelope frequency since changing the second harmonic frequencies will affect the in-band response of the amplifier.

This project has also compared the effects of adding the traps at either the input or the output of the DA. Placing traps at the input results in an improvement of up to 3.9 dB at the higher frequencies (2.5 GHz and 3.0 GHz). The linearity remains about the same at the lower frequencies. This is because the output trap only linearizes the C_{bc} nonlinearity and the effects can only be obvious when the g_m nonlinearities start to decrease at higher frequencies. Placing the trap at the input changes the source impedance as well as the base-emitter voltage. Since third order output current is dependent on the base-emitter voltage at the envelope frequencies, the traps cause the

voltage to drop, thus reducing the intermodulation current. Inserting traps at the input of the DA results in a linearity improvement of up to 7.4 dB throughout the measured band of 0.5 GHz to 3.0 GHz. Furthermore, the OIP3 is reported to achieve up to 19.2 dB above P_{1dB}.

These linearity improvements are significant because the other characteristics such as P_{1dB} and in-band S-parameters (gain and return loss) are not lowered. By varying the values of the LC trap, this project has also shown that the optimum trap values are those providing a small capacitive reactance at the envelope frequency. Two designs that utilize parallel ballasting are also shown to operate at lower current but still maintain the OIP3 above 33 dBm. By changing the $f_{spacing}$ (envelope frequency) between the two tones is varied while maintaining the center frequency at either 1, 2 or 3 GHz, improvement in OIP3 is still achieved with variation of less than 7%.

The drawback of the LC trap method is that it bring the device closer to instability since it provides low impedance at low frequencies. Nevertheless, with careful design and selection of the component values, the DA can still maintain unconditional stability. Stability test were performed for all the DA variants in this project and they are proven to be still stable even after the addition of the traps.

5.4 Future Work

In this thesis, the values for the LC trap are limited to commercial SMT values available in the market. Additional work can still be carried out to discover the effect that specific inductor and capacitor values have in terms of providing improvement in OIP3. For instance, the inductors might be printed on the testboard and can be designed to have values not found in the commercial SMTs (such as a 88 nH). This project has determined that a small capacitive reactance is the optimum termination but it has yet to quantify the extent of the improvement in terms of frequency. This is because the DA has been designed to roll-off at 3 GHz. Amplifiers with a high cut-off frequencies are needed to investigate this matter.

In this work, linearity measurements were made with the DA operating in the linear region and backed off from saturation. This region excludes the AM-AM and AM-PM distortion characteristics that occur near to saturation. Sources of distortion at high power levels are also known as the strong nonlinearities. Future work can also focus on strong nonlinearities of the HBT and tuning them out to provide broadband improvement at very high power levels.

Further effort can be channelled into improving broadband linearity for an FET. In addition, the linearity of FETs have been known to improve with the proper output termination but the mathematical analysis relating the output impedance with the third order intermodulation currents id not yet available. As mentioned earlier, this project is only a single step in the direction of creating a reconfigurable RF system. Much work is required at the system level to make reconfigurability possible. This includes combining the DA with improved broadband linearity with a tunable input filter.

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APPENDIX A

MATLAB CODES

```
function toc_reac
%MATLAB codes to obtain optimum termination for LC trap

gm1 = 1.0894;
gm2 = 20.9505;
gm3 = 268.5956;

g1 = 0.0158;
g2 = 0.3038;
g3 = 3.8953;

c1 = 3.5145e-12;
c2 = 6.2885e-11;
c3 = 8.0580e-10;

Vbe_w1 = 0.0825;
Vbe_w2 = 0.0825;

Rb = 4.65;
Re = 1.05;
r_pi = 1/0.0158;

Cdiff = 3.2682e-012;
Cdepl = 2.4629e-013;

ind = 0.2e-9;

%for 0.5GHz
freq1 = 0.495e9;
freq2 = 0.505e9;
w1 = 2*pi*freq1;
w2 = 2*pi*freq2;

X = 15;
Y=-500:10:500;

for num=1:1:101
cap(num) = i/((w2-w1)*(i*(w2-w1)*ind-Y(num)));

Zs_denv(num) = (i*(2*w2-w1)*ind)-(i/((2*w2-w1)*cap(num)));

Zs_2w2(num) = (i*(2*w2)*ind)-(i/((2*w2)*cap(num)));

Zpi_denv(num) = 1/(g1+i*(2*w2-w1)*Cdiff+i*(2*w2-w1)*Cdepl);

Zin_denv(num) = (Rb+Zpi_denv(num)+Re*(1+Zpi_denv(num)*gm1));

B(num) =
((Zs_denv(num)+Rb+Re)*Zpi_denv(num))/(Zin_denv(num)+Zs_denv(num));

C(num) = -
(((Zs_2w2(num)+Rb+Re)*(g2+i*2*w2*c2)+(Re*gm2))/(2*(1+(Zs_2w2(num)+Rb+
Re)*(g1+i*2*w2*c1)+Re*gm1))+(((X+Y(num)*i)+Rb+Re)*(g2+i*(w2-
w1)*c2)+Re*gm2)/(1+((X+Y(num)*i)+Rb+Re)*(g1+i*(w2-w1)*c1)+Re*gm1));
```

```
I(num) = B(num)*(((3/4)*(g1*gm3-g3*gm1)+C(num)*(g1*gm2-
g2*gm1))*Vbe_w2^2*conj(Vbe_w1))+B(num)*((3/4)*i*(2*w2-w1)*(c1*gm3-
c3*gm1)+i*(2*w2-w1)*+C(num)*(c1*gm2-
gm1*c2))*Vbe_w2^2*conj(Vbe_w1)+(Zpi_denv(num)/(Zin_denv(num)+Zs_denv(
num)))*(((3/4)*gm3+C(num)*gm2)*Vbe_w2^2*conj(Vbe_w1));
end
Z = 20*log(abs(I))
plot(Y,Z,'sb','LineWidth',2,'MarkerSize',12);
hold on;


%for 1GHz
freq1 = 0.995e9;
freq2 = 1.005e9;
w1 = 2*pi*freq1;
w2 = 2*pi*freq2;

X = 15;
Y=-500:10:500;

for num=1:1:101
cap(num) = i/((w2-w1)*(i*(w2-w1)*ind-Y(num)));

Zs_denv(num) = (i*(2*w2-w1)*ind)-(i/((2*w2-w1)*cap(num)));

Zs_2w2(num) = (i*(2*w2)*ind)-(i/((2*w2)*cap(num)));

Zpi_denv(num) = 1/(g1+i*(2*w2-w1)*Cdiff+i*(2*w2-w1)*Cdepl);

Zin_denv(num) = (Rb+Zpi_denv(num)+Re*(1+Zpi_denv(num)*gm1));

B(num) =
((Zs_denv(num)+Rb+Re)*Zpi_denv(num))/(Zin_denv(num)+Zs_denv(num));

C(num) = -
(((Zs_2w2(num)+Rb+Re)*(g2+i*2*w2*c2)+(Re*gm2))/(2*(1+(Zs_2w2(num)+Rb+
Re)*(g1+i*2*w2*c1)+Re*gm1))+(((X+Y(num)*i)+Rb+Re)*(g2+i*(w2-
w1)*c2)+Re*gm2)/(1+((X+Y(num)*i)+Rb+Re)*(g1+i*(w2-w1)*c1)+Re*gm1));
I(num) = B(num)*(((3/4)*(g1*gm3-g3*gm1)+C(num)*(g1*gm2-
g2*gm1))*Vbe_w2^2*conj(Vbe_w1))+B(num)*((3/4)*i*(2*w2-w1)*(c1*gm3-
c3*gm1)+i*(2*w2-w1)*+C(num)*(c1*gm2-
gm1*c2))*Vbe_w2^2*conj(Vbe_w1)+(Zpi_denv(num)/(Zin_denv(num)+Zs_denv(
num)))*(((3/4)*gm3+C(num)*gm2)*Vbe_w2^2*conj(Vbe_w1));
end
Z = 20*log(abs(I));
plot(Y,Z,'^k','LineWidth',2,'MarkerSize',12);


%for 1.5GHz
freq1 = 1.495e9;
freq2 = 1.505e9;
w1 = 2*pi*freq1;
w2 = 2*pi*freq2;

X = 15;
Y=-500:10:500;
```

```
for num=1:1:101
cap(num) = i/((w2-w1)*(i*(w2-w1)*ind-Y(num)));

Zs_denv(num) = (i*(2*w2-w1)*ind)-(i/((2*w2-w1)*cap(num)));

Zs_2w2(num) = (i*(2*w2)*ind)-(i/((2*w2)*cap(num)));

Zpi_denv(num) = 1/(g1+i*(2*w2-w1)*Cdiff+i*(2*w2-w1)*Cdepl);

Zin_denv(num) = (Rb+Zpi_denv(num)+Re*(1+Zpi_denv(num)*gm1));

B(num) =
((Zs_denv(num)+Rb+Re)*Zpi_denv(num))/(Zin_denv(num)+Zs_denv(num));

C(num) = -
(((Zs_2w2(num)+Rb+Re)*(g2+i*2*w2*c2)+(Re*gm2))/(2*(1+(Zs_2w2(num)+Rb+
Re)*(g1+i*2*w2*c1)+Re*gm1))+(((X+Y(num)*i)+Rb+Re)*(g2+i*(w2-
w1)*c2)+Re*gm2)/(1+((X+Y(num)*i)+Rb+Re)*(g1+i*(w2-w1)*c1)+Re*gm1));
I(num) = B(num)*(((3/4)*(g1*gm3-g3*gm1)+C(num)*(g1*gm2-
g2*gm1))*Vbe_w2^2*conj(Vbe_w1))+B(num)*((3/4)*i*(2*w2-w1)*(c1*gm3-
c3*gm1)+i*(2*w2-w1)*+C(num)*(c1*gm2-
gm1*c2))*Vbe_w2^2*conj(Vbe_w1)+(Zpi_denv(num)/(Zin_denv(num)+Zs_denv(
num)))*(((3/4)*gm3+C(num)*gm2)*Vbe_w2^2*conj(Vbe_w1));
end
Z = 20*log(abs(I));
plot(Y,Z,'or','LineWidth',2,'MarkerSize',12);


%for 2GHz
freq1 = 1.995e9;
freq2 = 2.005e9;
w1 = 2*pi*freq1;
w2 = 2*pi*freq2;

X = 15;
Y=-500:10:500;

for num=1:1:101
cap(num) = i/((w2-w1)*(i*(w2-w1)*ind-Y(num)));

Zs_denv(num) = (i*(2*w2-w1)*ind)-(i/((2*w2-w1)*cap(num)));

Zs_2w2(num) = (i*(2*w2)*ind)-(i/((2*w2)*cap(num)));

Zpi_denv(num) = 1/(g1+i*(2*w2-w1)*Cdiff+i*(2*w2-w1)*Cdepl);

Zin_denv(num) = (Rb+Zpi_denv(num)+Re*(1+Zpi_denv(num)*gm1));

B(num) =
((Zs_denv(num)+Rb+Re)*Zpi_denv(num))/(Zin_denv(num)+Zs_denv(num));

C(num) = -
(((Zs_2w2(num)+Rb+Re)*(g2+i*2*w2*c2)+(Re*gm2))/(2*(1+(Zs_2w2(num)+Rb+
```

```
Re)*(g1+i*2*w2*c1)+Re*gm1))+(((X+Y(num)*i)+Rb+Re)*(g2+i*(w2-
w1)*c2)+Re*gm2)/(1+((X+Y(num)*i)+Rb+Re)*(g1+i*(w2-w1)*c1)+Re*gm1));
I(num) = B(num)*(((3/4)*(g1*gm3-g3*gm1)+C(num)*(g1*gm2-
g2*gm1))*Vbe_w2^2*conj(Vbe_w1))+B(num)*((3/4)*i*(2*w2-w1)*(c1*gm3-
c3*gm1)+i*(2*w2-w1)*+C(num)*(c1*gm2-
gm1*c2))*Vbe_w2^2*conj(Vbe_w1)+(Zpi_denv(num)/(Zin_denv(num)+Zs_denv(
num)))*(((3/4)*gm3+C(num)*gm2)*Vbe_w2^2*conj(Vbe_w1));
end
Z = 20*log(abs(I));
plot(Y,Z,'xb','LineWidth',2,'MarkerSize',14);


%for 2.5GHz
freq1 = 2.495e9;
freq2 = 2.505e9;
w1 = 2*pi*freq1;
w2 = 2*pi*freq2;

X = 15;
Y=-500:10:500;

for num=1:1:101
cap(num) = i/((w2-w1)*(i*(w2-w1)*ind-Y(num)));

Zs_denv(num) = (i*(2*w2-w1)*ind)-(i/((2*w2-w1)*cap(num)));

Zs_2w2(num) = (i*(2*w2)*ind)-(i/((2*w2)*cap(num)));

Zpi_denv(num) = 1/(g1+i*(2*w2-w1)*Cdiff+i*(2*w2-w1)*Cdepl);

Zin_denv(num) = (Rb+Zpi_denv(num)+Re*(1+Zpi_denv(num)*gm1));

B(num) =
((Zs_denv(num)+Rb+Re)*Zpi_denv(num))/(Zin_denv(num)+Zs_denv(num));

C(num) = -
(((Zs_2w2(num)+Rb+Re)*(g2+i*2*w2*c2)+(Re*gm2))/(2*(1+(Zs_2w2(num)+Rb+
Re)*(g1+i*2*w2*c1)+Re*gm1))+(((X+Y(num)*i)+Rb+Re)*(g2+i*(w2-
w1)*c2)+Re*gm2)/(1+((X+Y(num)*i)+Rb+Re)*(g1+i*(w2-w1)*c1)+Re*gm1));
I(num) = B(num)*(((3/4)*(g1*gm3-g3*gm1)+C(num)*(g1*gm2-
g2*gm1))*Vbe_w2^2*conj(Vbe_w1))+B(num)*((3/4)*i*(2*w2-w1)*(c1*gm3-
c3*gm1)+i*(2*w2-w1)*+C(num)*(c1*gm2-
gm1*c2))*Vbe_w2^2*conj(Vbe_w1)+(Zpi_denv(num)/(Zin_denv(num)+Zs_denv(
num)))*(((3/4)*gm3+C(num)*gm2)*Vbe_w2^2*conj(Vbe_w1));
end
Z = 20*log(abs(I));
plot(Y,Z,'-k','LineWidth',3,'MarkerSize',12);


%for 3GHz
freq1 = 2.995e9;
freq2 = 3.005e9;
w1 = 2*pi*freq1;
w2 = 2*pi*freq2;

X = 15;
```

```
Y=-500:10:500;

for num=1:1:101
cap(num) = i/((w2-w1)*(i*(w2-w1)*ind-Y(num)));

Zs_denv(num) = (i*(2*w2-w1)*ind)-(i/((2*w2-w1)*cap(num)));

Zs_2w2(num) = (i*(2*w2)*ind)-(i/((2*w2)*cap(num)));

Zpi_denv(num) = 1/(g1+i*(2*w2-w1)*Cdiff+i*(2*w2-w1)*Cdepl);

Zin_denv(num) = (Rb+Zpi_denv(num)+Re*(1+Zpi_denv(num)*gm1));

B(num) =
((Zs_denv(num)+Rb+Re)*Zpi_denv(num))/(Zin_denv(num)+Zs_denv(num));

C(num) = -
(((Zs_2w2(num)+Rb+Re)*(g2+i*2*w2*c2)+(Re*gm2))/(2*(1+(Zs_2w2(num)+Rb+
Re)*(g1+i*2*w2*c1)+Re*gm1))+(((X+Y(num)*i)+Rb+Re)*(g2+i*(w2-
w1)*c2)+Re*gm2)/(1+((X+Y(num)*i)+Rb+Re)*(g1+i*(w2-w1)*c1)+Re*gm1));
I(num) = B(num)*(((3/4)*(g1*gm3-g3*gm1)+C(num)*(g1*gm2-
g2*gm1))*Vbe_w2^2*conj(Vbe_w1))+B(num)*((3/4)*i*(2*w2-w1)*(c1*gm3-
c3*gm1)+i*(2*w2-w1)*+C(num)*(c1*gm2-
gm1*c2))*Vbe_w2^2*conj(Vbe_w1)+(Zpi_denv(num)/(Zin_denv(num)+Zs_denv(
num)))*(((3/4)*gm3+C(num)*gm2)*Vbe_w2^2*conj(Vbe_w1));
end
Z = 20*log(abs(I));
plot(Y,Z,'--r','LineWidth',3,'MarkerSize',12);
```

APPENDIX B

STABILITY SIMULATION RESULTS

Table C.1 μ-factor for DA1 baseline and with LC trap

freq	DA1_base_stability..Mu1	DA1_trap_stability..Mu1
10.00 MHz	1.037	1.003
20.00 MHz	1.126	1.046
30.00 MHz	1.231	1.119
40.00 MHz	1.329	1.183
50.00 MHz	1.411	1.234
60.00 MHz	1.480	1.274
70.00 MHz	1.538	1.307
80.00 MHz	1.589	1.336
90.00 MHz	1.637	1.362
100.0 MHz	1.683	1.388
200.0 MHz	2.406	1.804
300.0 MHz	4.002	2.754
400.0 MHz	6.429	4.146
500.0 MHz	9.238	5.615
600.0 MHz	11.269	6.665
700.0 MHz	9.716	6.798
800.0 MHz	7.096	6.039
900.0 MHz	5.504	5.073
1.000 GHz	4.561	4.318
1.100 GHz	3.998	3.818
1.200 GHz	3.673	3.517
1.300 GHz	3.509	3.360
1.400 GHz	3.453	3.305
1.500 GHz	3.473	3.322
1.600 GHz	3.546	3.392
1.700 GHz	3.658	3.501
1.800 GHz	3.798	3.640
1.900 GHz	3.964	3.806
2.000 GHz	4.152	3.998
2.100 GHz	4.366	4.218
2.200 GHz	4.607	4.470
2.300 GHz	4.878	4.759
2.400 GHz	5.175	5.085
2.500 GHz	5.453	5.416
2.600 GHz	5.510	5.542
2.700 GHz	5.372	5.386
2.800 GHz	5.432	5.411
2.900 GHz	5.821	5.765
3.000 GHz	6.614	6.524

Table C.2 μ-factor for DA2 baseline and with LC trap

freq	DA2_base_stability..Mu1	DA2_trap_stability..Mu1
10.00 MHz	1.037	1.003
20.00 MHz	1.126	1.047
30.00 MHz	1.230	1.120
40.00 MHz	1.326	1.184
50.00 MHz	1.408	1.235
60.00 MHz	1.474	1.275
70.00 MHz	1.530	1.308
80.00 MHz	1.579	1.336
90.00 MHz	1.624	1.361
100.0 MHz	1.666	1.385
200.0 MHz	2.226	1.726
300.0 MHz	3.145	2.348
400.0 MHz	4.170	3.133
500.0 MHz	5.085	3.963
600.0 MHz	5.773	4.803
700.0 MHz	5.947	5.681
800.0 MHz	4.955	6.202
900.0 MHz	3.883	4.240
1.000 GHz	3.260	3.378
1.100 GHz	2.934	2.961
1.200 GHz	2.790	2.771
1.300 GHz	2.758	2.710
1.400 GHz	2.795	2.724
1.500 GHz	2.872	2.783
1.600 GHz	2.968	2.866
1.700 GHz	3.070	2.961
1.800 GHz	3.170	3.059
1.900 GHz	3.259	3.152
2.000 GHz	3.324	3.229
2.100 GHz	3.345	3.271
2.200 GHz	3.292	3.251
2.300 GHz	3.151	3.143
2.400 GHz	2.975	2.987
2.500 GHz	2.875	2.890
2.600 GHz	2.932	2.945
2.700 GHz	3.198	3.203
2.800 GHz	3.709	3.700
2.900 GHz	4.500	4.465
3.000 GHz	5.591	5.530

Table C.3 μ-factor for DA3 baseline and with LC trap

freq	DA3_base_stability..Mu1	DA3_trap_stability..Mu1
10.00 MHz	1.037	1.003
20.00 MHz	1.126	1.047
30.00 MHz	1.231	1.119
40.00 MHz	1.328	1.184
50.00 MHz	1.409	1.235
60.00 MHz	1.477	1.275
70.00 MHz	1.533	1.307
80.00 MHz	1.582	1.335
90.00 MHz	1.628	1.360
100.0 MHz	1.671	1.384
200.0 MHz	2.363	1.783
300.0 MHz	4.254	2.869
400.0 MHz	8.495	4.868
500.0 MHz	13.498	6.805
600.0 MHz	9.035	6.633
700.0 MHz	6.612	5.597
800.0 MHz	5.384	4.780
900.0 MHz	4.652	4.222
1.000 GHz	4.180	3.843
1.100 GHz	3.867	3.587
1.200 GHz	3.662	3.420
1.300 GHz	3.535	3.320
1.400 GHz	3.467	3.270
1.500 GHz	3.442	3.261
1.600 GHz	3.453	3.284
1.700 GHz	3.492	3.334
1.800 GHz	3.558	3.410
1.900 GHz	3.649	3.512
2.000 GHz	3.769	3.643
2.100 GHz	3.925	3.810
2.200 GHz	4.129	4.026
2.300 GHz	4.394	4.302
2.400 GHz	4.719	4.638
2.500 GHz	5.061	4.993
2.600 GHz	5.312	5.268
2.700 GHz	5.435	5.423
2.800 GHz	5.508	5.529
2.900 GHz	5.583	5.640
3.000 GHz	5.668	5.766

Table C.4 μ-factor for DA4 baseline and with LC trap

freq	DA4_base_stability..Mu1	DA4_trap_stability..Mu1
10.00 MHz	1.037	1.003
20.00 MHz	1.125	1.047
30.00 MHz	1.228	1.121
40.00 MHz	1.322	1.185
50.00 MHz	1.401	1.236
60.00 MHz	1.465	1.275
70.00 MHz	1.518	1.307
80.00 MHz	1.564	1.333
90.00 MHz	1.605	1.357
100.0 MHz	1.645	1.379
200.0 MHz	2.250	1.733
300.0 MHz	4.188	2.852
400.0 MHz	10.799	5.710
500.0 MHz	13.352	8.782
600.0 MHz	7.122	6.547
700.0 MHz	5.341	5.009
800.0 MHz	4.499	4.224
900.0 MHz	4.025	3.783
1.000 GHz	3.746	3.525
1.100 GHz	3.588	3.382
1.200 GHz	3.514	3.318
1.300 GHz	3.499	3.310
1.400 GHz	3.531	3.346
1.500 GHz	3.597	3.416
1.600 GHz	3.693	3.515
1.700 GHz	3.815	3.640
1.800 GHz	3.961	3.790
1.900 GHz	4.127	3.962
2.000 GHz	4.305	4.150
2.100 GHz	4.479	4.338
2.200 GHz	4.622	4.503
2.300 GHz	4.719	4.625
2.400 GHz	4.786	4.716
2.500 GHz	4.852	4.803
2.600 GHz	4.941	4.912
2.700 GHz	5.070	5.061
2.800 GHz	5.247	5.261
2.900 GHz	5.488	5.532
3.000 GHz	5.821	5.903

Table C.5 μ-factor for DA1 baseline and with LC trap

freq	DA1A_base_stability..Mu1	DA1A_trap_stability..Mu1
10.00 MHz	1.029	1.029
20.00 MHz	1.104	1.103
30.00 MHz	1.196	1.195
40.00 MHz	1.286	1.282
50.00 MHz	1.367	1.358
60.00 MHz	1.437	1.421
70.00 MHz	1.500	1.474
80.00 MHz	1.556	1.518
90.00 MHz	1.608	1.555
100.0 MHz	1.657	1.585
200.0 MHz	2.084	1.718
300.0 MHz	2.535	2.262
400.0 MHz	3.440	3.884
500.0 MHz	4.442	5.768
600.0 MHz	5.602	7.765
700.0 MHz	6.723	9.453
800.0 MHz	7.886	10.972
900.0 MHz	8.911	11.993
1.000 GHz	9.870	12.647
1.100 GHz	10.471	12.502
1.200 GHz	10.605	11.680
1.300 GHz	10.171	10.528
1.400 GHz	9.412	9.415
1.500 GHz	8.622	8.525
1.600 GHz	7.946	7.840
1.700 GHz	7.451	7.366
1.800 GHz	7.112	7.050
1.900 GHz	6.926	6.884
2.000 GHz	6.854	6.828
2.100 GHz	6.907	6.895
2.200 GHz	7.068	7.066
2.300 GHz	7.348	7.355
2.400 GHz	7.731	7.745
2.500 GHz	8.215	8.234
2.600 GHz	8.707	8.724
2.700 GHz	8.938	8.943
2.800 GHz	8.605	8.597
2.900 GHz	7.893	7.884
3.000 GHz	7.211	7.206

Table C.6 μ-factor for DA1B baseline and with LC trap

freq	DA1B_base_stability..Mu1	DA1B_trap_stability..Mu1
10.00 MHz	1.029	1.029
20.00 MHz	1.104	1.103
30.00 MHz	1.196	1.195
40.00 MHz	1.286	1.282
50.00 MHz	1.367	1.358
60.00 MHz	1.437	1.422
70.00 MHz	1.500	1.476
80.00 MHz	1.556	1.520
90.00 MHz	1.608	1.557
100.0 MHz	1.657	1.588
200.0 MHz	2.084	1.723
300.0 MHz	2.534	2.257
400.0 MHz	3.438	3.911
500.0 MHz	4.437	5.847
600.0 MHz	5.597	7.871
700.0 MHz	6.720	9.538
800.0 MHz	7.891	11.001
900.0 MHz	8.934	11.957
1.000 GHz	9.921	12.562
1.100 GHz	10.553	12.412
1.200 GHz	10.705	11.618
1.300 GHz	10.256	10.494
1.400 GHz	9.464	9.396
1.500 GHz	8.647	8.511
1.600 GHz	7.955	7.829
1.700 GHz	7.455	7.358
1.800 GHz	7.115	7.044
1.900 GHz	6.932	6.883
2.000 GHz	6.867	6.835
2.100 GHz	6.929	6.910
2.200 GHz	7.103	7.094
2.300 GHz	7.399	7.399
2.400 GHz	7.804	7.811
2.500 GHz	8.312	8.326
2.600 GHz	8.819	8.834
2.700 GHz	9.011	9.017
2.800 GHz	8.589	8.583
2.900 GHz	7.827	7.818
3.000 GHz	7.130	7.123

Table C.7 μ-factor for DA4A baseline and with LC trap

freq	DA4A_base_stability..Mu1	DA4A_trap_stability..Mu1
10.00 MHz	1.029	1.029
20.00 MHz	1.104	1.103
30.00 MHz	1.196	1.194
40.00 MHz	1.285	1.281
50.00 MHz	1.365	1.356
60.00 MHz	1.434	1.419
70.00 MHz	1.496	1.471
80.00 MHz	1.551	1.514
90.00 MHz	1.601	1.549
100.0 MHz	1.648	1.577
200.0 MHz	2.026	1.628
300.0 MHz	2.379	2.004
400.0 MHz	3.093	3.422
500.0 MHz	3.834	4.987
600.0 MHz	4.649	6.417
700.0 MHz	5.378	7.395
800.0 MHz	6.088	8.121
900.0 MHz	6.666	8.500
1.000 GHz	7.184	8.729
1.100 GHz	7.518	8.682
1.200 GHz	7.677	8.435
1.300 GHz	7.591	7.990
1.400 GHz	7.323	7.465
1.500 GHz	6.928	6.938
1.600 GHz	6.516	6.475
1.700 GHz	6.161	6.113
1.800 GHz	5.895	5.854
1.900 GHz	5.724	5.695
2.000 GHz	5.634	5.617
2.100 GHz	5.625	5.619
2.200 GHz	5.686	5.688
2.300 GHz	5.803	5.812
2.400 GHz	5.951	5.964
2.500 GHz	6.084	6.098
2.600 GHz	6.122	6.131
2.700 GHz	5.965	5.967
2.800 GHz	5.631	5.628
2.900 GHz	5.223	5.221
3.000 GHz	4.875	4.874